

# I3T80

## Process Technology

# I3T80: 0.35 $\mu\text{m}$ Process Technology



ON Semiconductor®

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### Overview

Providing the density of a 0.35  $\mu\text{m}$  digital process, analog/mixed-signal capability and high voltage, the ON Semiconductor Intelligent Interface Technology I3T80 process is the answer to the need for increased digital content in a mixed-signal and/or high voltage environment. Featuring high voltage devices up to 80 V as well as digital and analog operation at 3.3 V, the I3T80 process family features a wide range of capabilities in a single IC.

### Features

- 3 to 5 Metal Layers
- Metal to Metal (MIM) Linear Capacitors
- High, Medium, and Low Resistivity Polysilicon Resistors
- Floating High-Voltage NDMOS and PDMOS Transistors
- Floating Medium-Voltage NDMOS Transistors
- Floating High- and Low-Voltage Diodes
- Medium-Voltage NPN Bipolar Transistors
- Medium-Voltage PNP Bipolar Transistors (Collector Grounded, High and Low Gain)
- Zener Zap Diode for OTP
- Buried Zener Diode for Clamping
- Polysilicon Clamping Diode
- High- and Medium-Voltage Floating Metal Capacitors
- Deep N+ Doped Guard Rings

### PROCESS CHARACTERISTICS

Operating Voltage	3.3 V
Substrate Material	N-epitaxy on P-sub, Retrograde Wells
Drawn Transistor Length	0.35 $\mu\text{m}$
Gate Oxide Thickness	7.0 nm
Contact/Via Size	0.4 $\mu\text{m}$
Contacted Gate Pitch	1.3 $\mu\text{m}$
Top Metal Thickness	1020 nm
Metal Pitch	
Metal 1	1.0 $\mu\text{m}$
Metal 2	1.1 $\mu\text{m}$
Top Metal	1.4 $\mu\text{m}$
Contacted Metal Pitch	
Metal 1/ CNT	1.1 $\mu\text{m}$
Metal 1/ Via 1	1.2 $\mu\text{m}$
Metal 2 to Top 1 / Via	1.2 $\mu\text{m}$
Metal Composition	Al/Cu
Isolation	LOCOS
ILD Planarization	USG/BPTEOS+CMP
IMD Planarization	HDP/PETEOS+CMP

### SAMPLE PROCESS OPTIONS

	Mask Layers
3 Metal, 80 V, MIMC, HIPO, OTP	23
4 Metal, 80 V, MIMC, HIPO, OTP	25
5 Metal, 80 V, MIMC, HIPO, OTP, Flash EEPROM	28

**DEVICE CHARACTERISTICS**

All Values Typical at 25°C

**LOW-VOLTAGE TRANSISTORS**

<b>NMOS Transistor</b>	<b>Typical Value</b>	<b>Units</b>
Vt (10/0.35, linear extrapolated)	0.59	V
Vmax = Vbd	3.6	V
IDS (10/0.35, Vds = Vgs = 3.3 V)	530	μA/μm
<b>PMOS Transistor</b>	<b>Typical Value</b>	<b>Units</b>
Vt (10/0.35, linear extrapolated)	-0.57	V
Vmax = Vbd	-3.6	V
IDS (10/0.35, Vds = Vgs = 3.3 V)	-250	μA/μm

**HIGH-VOLTAGE TRANSISTORS**

<b>Floating NMOS @ 80 V</b>	<b>Typical Value</b>	<b>Units</b>
Vt (10/0.35, linear extrapolated)	0.59	V
Vmax = Vfloat to P-substrate	80	V
Vmax = Vbd	3.6	V
IDS (10/0.35, Vds = Vgs = 3.3 V)	530	μA/μm
<b>Floating PMOS @ 80 V</b>	<b>Typical Value</b>	<b>Units</b>
Vt (10/0.35, linear extrapolated)	-0.57	V
Vmax = Vfloat to P-substrate	80	V
Vmax = Vbd	-3.6	V
IDS (10/0.35, Vds = Vgs = 3.3 V)	-250	μA/μm
<b>Floating NDMOS for Switching Application: VFNDM80</b>	<b>Typical Value</b>	<b>Units</b>
Vt	0.54	V
Vmax = Vbd (higher if self protected)	70	V
Vgsmax (full lifetime)	3.6	V
Ids (Vds = 40, Vgs = 1.5 V)	100	μA/μm
Ron*Area (block of 16 fingers) Without isolation With isolation	180 260	mΩ*mm <sup>2</sup>
<b>Floating NDMOS for Analog Application: VFNDM80A</b>	<b>Typical Value</b>	<b>Units</b>
Vt	0.56	V
Vmax = Vbd (higher if self protected)	70	V
Vgsmax (full lifetime)	3.6	V
Ids (Vds = 40, Vgs = 1.5 V)	70	μA/μm
Ron*Area (block of 16 fingers) Without isolation With isolation	250 325	mΩ*mm <sup>2</sup>

<b>Floating Medium Voltage NDMOS</b>	<b>Typical Value</b>	<b>Units</b>
Vt	0.58	V
Vmax = Vbd	14	V
Vgsmax (full lifetime)	3.6	V
Ids (Vds = 10 V, Vgs = 3.3 V)	300	μA/μm
Ron*Area	31	mΩ*mm <sup>2</sup>
<b>Floating HV PMOS: LFPDM80</b>	<b>Typical Value</b>	<b>Units</b>
Vt (W = 40 mm)	-0.56	V
Vmax = Vbd	-70	V
Vgsmax (full lifetime)	-3.6	V
Ids (Vds = 40 V, Vgs = 1.5 V)	18.5	μA/μm
Ron*Area	280	mΩ*mm <sup>2</sup>
<b>Floating PDMOS: LFPDMS</b>	<b>Typical Value</b>	<b>Units</b>
Vt	-0.56	V
Vmax = Vbd	-5.5	V
Vgsmax	-3.6	V
Ids (Vds = 5 V, Vgs = 3.3 V)	96	μA/μm

**DIODES**

<b>Zener Diode: PBZD (a = 2 μm)</b>	<b>Typical Value</b>	<b>Units</b>
Vz @ 100 μA	4.6	V
Rzener	45	Ω
Ileak @ Vz = 0.5 V	200	nA
<b>Zapping Zener Diode for OTP: UZZD</b>	<b>Typical Value</b>	<b>Units</b>
Vz @ 1 A	1.5	V
Vbd @ 10 mA	4.5	V
Ileak_max @ Vz = 1 V	1.4	mA
<b>Floating High Voltage Diode: FID80</b>	<b>Typical Value</b>	<b>Units</b>
Vak_reverse, Ia = 100 nA	> 80	V
Vak_forw, Ik = 100 μA	0.79	V
Isub/IA, Va = 0.7 V	0.5	%
<b>Poly Diode for Gate Clamping: POLYD</b>	<b>Typical Value</b>	<b>Units</b>
Vreverse @ Ia = 10 μA	6.8	V
Ileak/W @ Vrev = 3.6 V	< 20	nA/μm

## BIPOLAR TRANSISTORS

<b>Vertical Medium-Voltage PNP: VPB (Parameter, E_area = 0.64 <math>\mu\text{m}^2</math>)</b>	<b>Typical Value</b>	<b>Units</b>
Hfe @ Ic = 10 $\mu\text{A}$	8	–
Bvceo @ Ic = 1 $\mu\text{A}$	–63	V
Bvces @ Ic = 1 $\mu\text{A}$	–67	V
Icmax	250	$\mu\text{A}$
<b>Vertical Medium-Voltage “High-Gain” PNP Transistor: VPHB (Parameter, E_area = 0.64 <math>\mu\text{m}^2</math>)</b>	<b>Typical Value</b>	<b>Units</b>
Hfe @ Ic = 100 nA	115	–
Bvceo  @ Ic = 1 $\mu\text{A}$	> 80	V
Bvces  @ Ic = 1 $\mu\text{A}$	> 100	V
Icmax	250	$\mu\text{A}$
<b>Medium-Voltage NPN (Parameter, E_area = 16 <math>\mu\text{m}^2</math>)</b>	<b>Typical Value</b>	<b>Units</b>
Hfe max	120	–
Bvceo @ Ic = 1 $\mu\text{A}$	23	V
Bvces @ Ic = 1 $\mu\text{A}$	> 80	V
Vearly	> 70	V

## CAPACITORS (PARAMETER @ 25°C)

<b>Type (Maximum Voltage)</b>	<b>Typical Value</b>	<b>Units</b>
Metal2 / Metal2.5 Plate: MIMC (3.6 V)	1.5	fF/ $\mu\text{m}^2$
Metal1 / Metal3 Plate (80 V)	0.1	fF/ $\mu\text{m}^2$
Poly / Metal3 Plate (80 V)	0.14	fF/ $\mu\text{m}^2$
Metal1 / Metal3 Bar (80 V)	0.26	aF/ $\mu\text{m}$ / finger
Poly / Metal3 Bar (80 V)	0.33	aF/ $\mu\text{m}$ / finger

## RESISTORS (PARAMETER @ 25°C)

<b>Resistor Type</b>	<b>Typical Value</b>	<b>Units</b>
High-Resistance Poly: HIPO	975	$\Omega$ /square
Salicided P+ Poly: LOPOR	2.4	$\Omega$ /square
Unsalicided P+ Poly: PPOLR	240	$\Omega$ /square
Unsalicided P+ in Mwell	64	$\Omega$ /square
Unsalicided N+ Poly: NPOLR	292	$\Omega$ /square
Unsalicided N+ in Pwell	47.5	$\Omega$ /square
Nwell under FOX (field oxide)	958	$\Omega$ /square
Nwell in AA (active area)	800	$\Omega$ /square
Pwell in AA (active area)	1755	$\Omega$ /square

## LIBRARIES

<b>Standard Cell</b>	
<b>Ultra High Density Core Shell</b>	pn sum: 2.0
	Area of 2-input nand (na21): 38.88 $\mu\text{m}^2$
	Gate density (na21 @ 100% utilization): 25.72 k gates/ $\text{mm}^2$
	Scan Flop density (scan flops @ 100% utilization): 3.215 k ff/ $\text{mm}^2$
Average power (@ 3.3 V): 0.2929 $\mu\text{W}/\text{MHz}/\text{gate}$	
<b>Standard I/O</b>	
<b>Fat Pad I/O Library (for core limited designs)</b>	190.80 $\mu\text{m}$ min in-line pad pitch
	203.40 $\mu\text{m}$ pad height
<b>Tall Pad I/O Library (for pad limited designs)</b>	97.20 $\mu\text{m}$ min in-line pad pitch
	374.40 $\mu\text{m}$ pad height

## MEMORY OPTIONS

<b>RAM</b>	
<b>Synchronous High Speed / High Temp Single Port SRAM</b>	Minimum: 16 words x 2 bits
	Maximum: 128 k bits (i.e: 16 k words x 8 bits, 8 k words x 16 bits, ...)
<b>Synchronous High Speed / High Temp Dual Port SRAM</b>	Minimum: 16 words x 2 bits
	Maximum: 128 k bits (i.e: 16 k words x 8 bits, 8 k words x 16 bits, ...)
<b>Low Power Synchronous SRAM</b>	Minimum: 64 words x 4 bits
	Maximum: 128 k bits (i.e: 16 k words x 8 bits, 8 k words x 16 bits, ...)
<b>ROM</b>	
<b>Synchronous High Speed / High Temp Diffusion ROM</b>	Minimum: 256 words x 4 bits
	Maximum: 512 k bits (i.e: 64 k words x 8 bits, 32 k words x 16 bits, ...)
<b>Low Power Synchronous Via Programmable ROM</b>	Minimum: 256 words x 4 bits
	Maximum: 512 k bits (i.e: 64 k words x 8 bits, 32 k words x 16 bits, ...)
<b>Non-Volatile Memory</b>	
<b>OTP – One Time Programmable</b>	Fuse: Zener Diode optimized for low power zapping
	Both Serial and Parallel Output Capability
	In field programming available
	Vector: Up to 320 bits

## CAD TOOL COMPATIBILITY

<b>Digital Design</b>	Synopsys Design Compiler
	Cadence Verilog
<b>Analog Design</b>	Cadence DFII (4.4.6)
	Spectre
<b>Place and Route</b>	Synopsys Apollo
	Cadence Silicon Ensemble
<b>Physical Verification</b>	Mentor Graphics Calibre

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