ON Semiconductor

Is Now

To learn more about onsemi™, please visit our website at
www.onsemi.com

onsemi and onsemi and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi** product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner. Other names and brands may be claimed as the property of others.

AND9033

Description of the ON Semiconductor MOSFET Model

ON Semiconductor®

http://onsemi.com

APPLICATION NOTE

Structure of MOSFET Model

Figure 1 shows the structure of ON Semiconductor's MOSFET Model. The MOSFET model includes the following components:

- level−1 static MOSFET model M1, nonlinear capacitance between gate and drain FI1 and FI2
- nonlinear capacitance between drain and source (included in D1)
- MOSFET body diode D1, internal gate resistance RG
- parasitic linear capacitance between gate and source (included in M1)
- parasitic linear capacitance between gate and drain (included in M1)
- parasitic package resistance of gate, drain, and source, and parasitic body resistance RDS. Parasitic inductance of the package is not included.

The ON Semiconductor MOSFET model shows excellent correlation with experimental results even though level−1 static MOSFET model is utilized. Higher static MOSFET models do not necessarily have higher accuracy if model parameters are not well characterized.

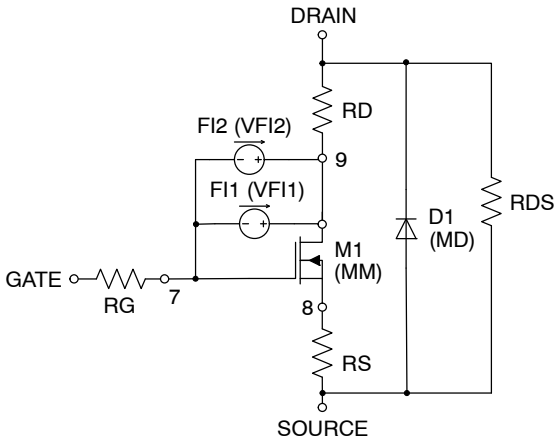


Figure 1. Structure of MOSFET Model

Level−1 MOSFET Model

In Figure 1, M1 is the main MOSFET. Note that voltage dependant capacitances are not included in M1. Only parasitic capacitances, such as gate−source overlay capacitance and gate−drain overlay capacitance, are included in M1. The structure of M1 is shown in Figure 2.

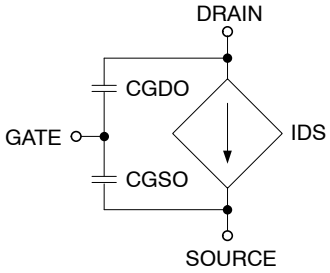


Figure 2. Structure of M1

In Figure 2, CGDO and CGSO are parasitic parameters, which are constants. IDS is a current source controlled by voltage V_{GS} and V_{DS}. The controlled current source is expressed by Equation 1.

$$\text{If } V_{GS} \le \text{VTO} \qquad \text{IDS} = 0 \qquad \text{(eq. 1)}$$

$$\text{If } V_{DS} \le V_{SAT}$$

$$\text{IDS} = \text{KP} \times \left((V_{GS} - \text{VTO}) \times V_{DS} - \frac{1}{2} V_{DS}^{2}\right)$$

$$\text{If } V_{DS} > V_{SAT}$$

$$\text{IDS} = \frac{1}{2} \times \text{KP} \times (V_{GS} - \text{VTO})^2 \times (1 + \text{LAMBDA} \times V_{DS})$$

Here,

$$V_{SAT} = V_{GS} - \text{VTO} \qquad \text{(eq. 2)}$$

Parameters of level−1 MOSFET model are:

VTO: Zero Bias Threshold Voltage
LAMBDA: Channel Length Modulation
KP: Transconductance Parameter
CGSO: Gate−Source Overlap Capacitance
CGDO: Gate−Drain Overlap Capacitance

Reverse Diode Model

In Figure 1, D1 is the MOSFET body diode. Both the diode reverse recovery loss and the power loss when operating in the third quadrant are captured by the diode. The structure of the body diode model is shown in Figure 3.

© Semiconductor Components Industries, LLC, 2011

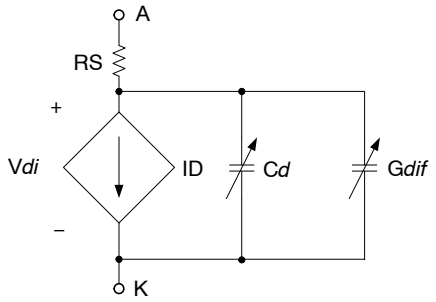


Figure 3. Structure of D1

In Figure 3, the current of controlled current source ID, which in fact is a pn junction diode without parasitics, is expressed by Equation 3.

$$I_D = IS \times \left(\exp\left(\frac{Vdi}{N \times V_{th}} \right) - 1 \right) \quad \text{(eq. 3)}$$

The depletion capacitance, Cd, is expressed by Equation 4.

$$\text{If } Vdi \le FC \times VJ \quad \text{(eq. 4)}$$

$$C_d = CJO \times \left(1 - \frac{V_{di}}{VJ} \right)^{-M}$$

$$\text{If } Vdi > FC \times VJ$$

$$C_d = CJO \times (1 - FC)^{-(1+M)} \times \left[1 - FC \times (1 + M) + M \times \frac{V_{di}}{VJ} \right]$$

The diffusion capacitance, Cdif, is expressed by Equation 5. Here, 'I' is the diode forward conducting DC current.

$$C_{dif} = TT \times \frac{dI}{dV_{di}} \quad \text{(eq. 5)}$$

For protection purpose, the breakdown current IB of D1 is expressed by Equation 6.

$$I_B = IBV \times \exp\left(- \frac{V_{di} + BV}{N \times V_{th}} \right) \quad \text{(eq. 6)}$$

Parameters of the reverse diode model are:

IS: Saturation Current
RS: Ohmic Resistance
N: Emission Coefficient
BV: Reverse Breakdown Voltage
IBV: Current at Reverse Breakdown
TT: Transit Time
CJO: Cross Junction Capacitance
VJ: Cross Junction Potential
M: Cross Junction Grading Coefficient
FC: Depletion Capacitance Coefficient

Parasitic Resistances

In Figure 1, RDS is the MOSFET body resistance. Rd is the drain ohmic resistance, RS is the source ohmic resistance, and Rg is the gate resistance.

Nonlinear Capacitance Model for Crss

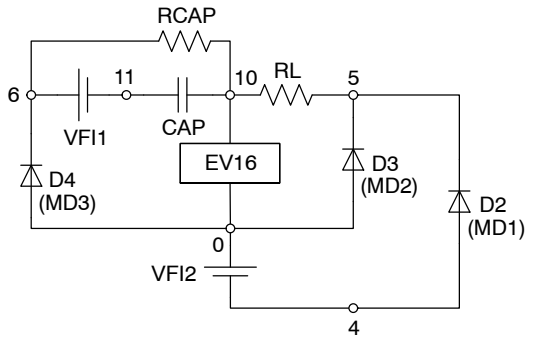
Based on Equation 3~6, one can see that D2 is a junction capacitor because its forward conducting DC current is extremely small. The junction capacitance of D2 is voltage dependant and is equal to Crss of MOSFET.

Parameters of diode D2 are:

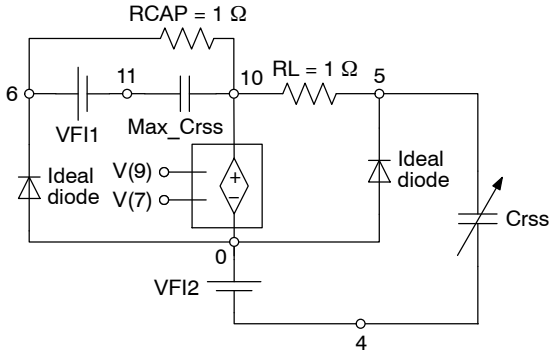
CJO: Crss Junction Capacitance
VJ: Crss Junction built−in potential
M: Crss Junction Exponential Factor
FC: FC of Crss Junction Capacitance

With parameter values specified in model, D3 and D4 have very small forward conducting voltage drop and very high turn−on and turn−off transition speed due to zero junction capacitance. Therefore, D3 and D4 model ideal diodes, which block reverse voltage with zero leakage current and conduct forward current with zero voltage drop.

Figure 4(a) is the control circuit of the controlled current sources FI1 and FI2. The current of controlled current source FI1 is the current flowing through zero−voltage source VFI1; the current of controlled current source FI2 is the current flowing through zero−voltage source VFI2.



(a) Control circuit of FI1 and FI2



(b) Analysis circuit of control circuit of FI1 and FI2

Figure 4. Gate−Drain Diode Schematic

Figure 4(b) is the analysis circuit of the control circuit for FI1 and FI2 shown in Figure 4(a). The voltage of node 10 is controlled by the voltage difference between node 9 and node 7, which is expressed by Equation 7.

$$V(10) = V(9) - V(7) \quad \text{(eq. 7)}$$

One can see that Max_Crss charges or discharges and the nonlinear capacitor Crss is shorted by an ideal diode when voltage V(9)<V(7). This process happens at the last instant of MOSFET switching ON and the first intant of MOSFET switching OFF. The nonlinear capacitor Crss charges or discharges and Max_Crss is blocked by another ideal diode when V(7)<V(9). This procedure happens when the drain−source voltage is increasing or decreasing. The capacitances Max_Crss and Crss function in a complimentary way. As a result, Max_Crss and Crss form the function of Crss in a complete switching cycle.

In fact, a nonlinear capacitor Crss connected between node 7 and node 9 in Figure 1 will work for a MOSFET model. However, splitting Crss into two capacitors, a constant capacitor Max_Crss and a nonlinear capacitor Crss, may improve convergence of the whole MOSFET model because the nonlinear behavior of Crss at low bias is significant. A constant capacitor Max_Crss will give good simulation accuracy while maintaining high convergence capability.

In Figure 5, Max_Crss simulates the gate charge Q3, where, gate−source voltage increases as gate charge increases. Crss simulates the charge Q2, which is called Miller charge.

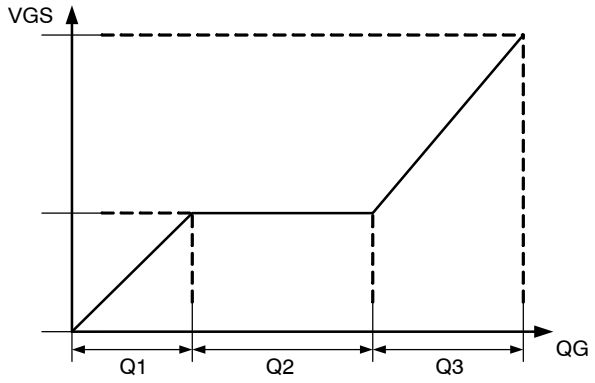


Figure 5. Total Gate Charge vs. Gate−source Voltage

Simulation Results

Simulated turn−on waveforms of MOSFET in a Buck converter circuit are shown in Figure 6.

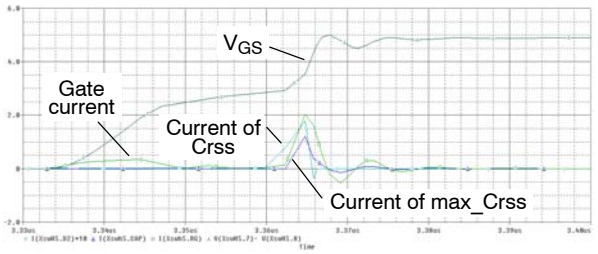


Figure 6. Simulated Turn−on Waveforms of MOSFET in a Buck Converter

Simulated turn−off waveforms of MOSFET in a Buck converter circuit are shown in Figure 7.

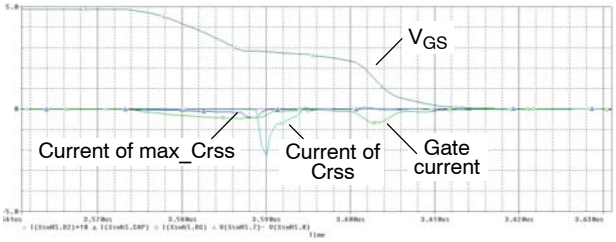


Figure 7. Simulated Turn−off Waveforms of MOSFET in a Buck Converter

References

[1] Tor A. Fjeldly, Trond Ytterdal, Michael S. Shur, ".Introduction to Device Modeling and Circuit Simulation." Wiley, John & Sons, ISBN−13: 9780471157786

[2] B. Van Zeghbroeck, "Principles for semiconductor devices," Prentice Hall; 1 edition (December 2009), ISBN−10: 0130409049

[3] "MOSFET models for VLSI circuit simulation: theory and practice" Springer−Verlag New York, Inc. Secaucus, NJ, USA ©1993, ISBN:0387823956

[4] Kraus, R.; Turkes, P.; Sigg, J., "Physics−based models of power semiconductor devices for the circuit simulator SPICE", Power Electronics Specialists Conference, 1998. PESC 98 Record. 29th Annual IEEE

[5] http://www.electronics−lab.com/downloads/schematic/013/tutorial/PSPCREF.pdf

[6] http://www.seas.upenn.edu/~jan/spice/PSpice_UserguideOrCAD.pdf

ON Semiconductor and ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

AND9033/D