High Efficiency 2 Phase Booster LED Driver for Automotive Front Lighting

NCV78902

The NCV78902 is a single-chip and high efficient 2 phase Booster LED Driver designed for automotive front lighting applications like high beam, low beam, DRL (daytime running light), turn indicator, fog light, static cornering, etc. The NCV78902 is in particular designed for high current LEDs and provides a complete solution to drive two LED strings of up-to 60 V with minimum of external components.

The device integrates a current-mode voltage booster controller, realizing a unique input current filter with a limited BOM. The available output voltage can be customized. Two devices NCV78902 can be combined and the booster circuits can operate together to function as a multiphase booster (2-phase, 3-phase, 4-phase) in order to further optimize the filtering effect of the booster and allow cost effective dimensioning for mid to high power LED systems.

Thanks to the SPI programmability, one single hardware configuration can support various application platforms.

Features

- Single Chip 2 Phase Booster Solution
- 2 Phase Current-mode Boost Controller
- Current Sensing on Shunt Resistors or MOSFETs' RDSon
- Active Input Filter with Low Current Ripple from Battery
- Low EMC Emission for LED Switching and Dimming
- High Overall Efficiency
- Minimum of External Components
- High Operating Frequencies to Reduce Inductor Sizes
- 4 MHz SPI Interface for Dynamic Control of System Parameters
- Fail Safe Operation (FSO) and Stand-Alone Modes Available
- ASIL B Compliant; AEC–Q100 Qualified and PPAP Capable
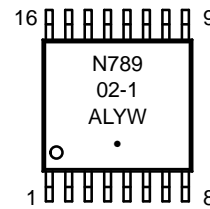- This Device is Pb-Free, Halide Free and are RoHS Compliant

Typical Applications

- High Beam, Low Beam
- Turn Indicator, DRL
- Position or Park Light
- Fog and Static Cornering
- Adaptive Driving Beam
- Pixel Applications
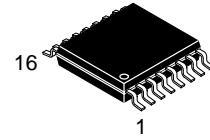
TSSOP–16 WB
CASE 948F

MARKING DIAGRAM

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N789
02-1
ALYW
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N78902-1 = Specific Device Code
A   = Assembly Location
L   = Wafer Lot
YW   = Year / Work Week
•   = Pb-Free Package

SAFETY DESIGN – ASIL B

ASIL B Product developed in compliance with ISO 26262 for which a complete safety package is available.

ORDERING INFORMATION

See detailed ordering and shipping information on page 36 of this data sheet.
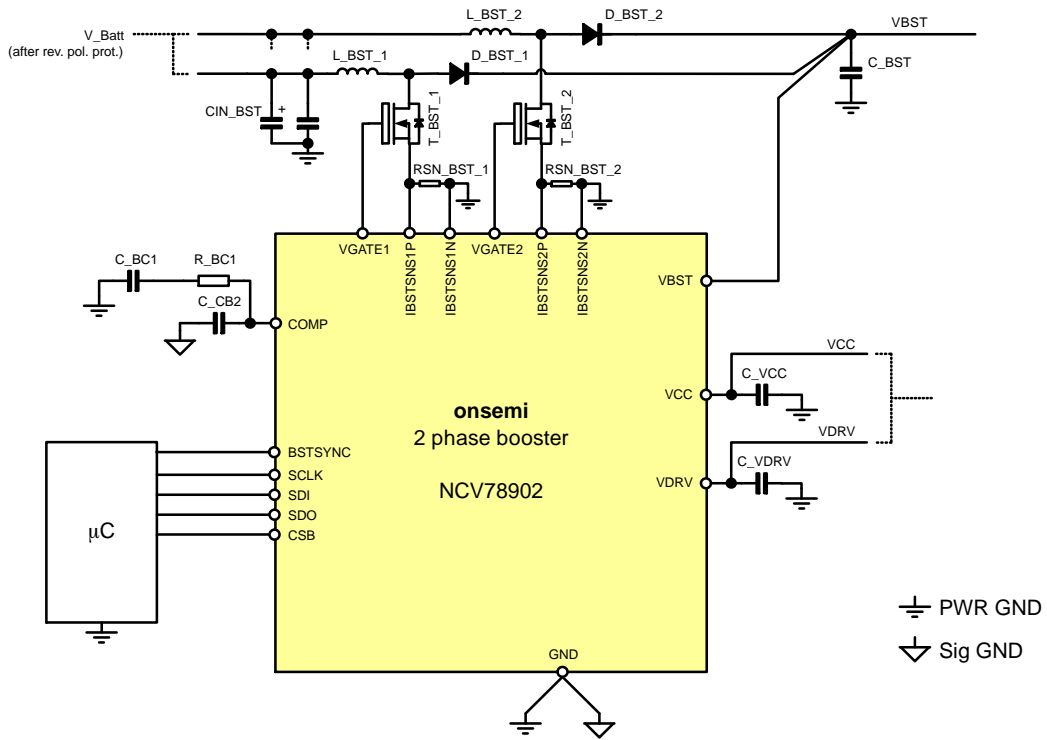
TYPICAL APPLICATION SCHEMATIC

Figure 1. Typical Application Schematic
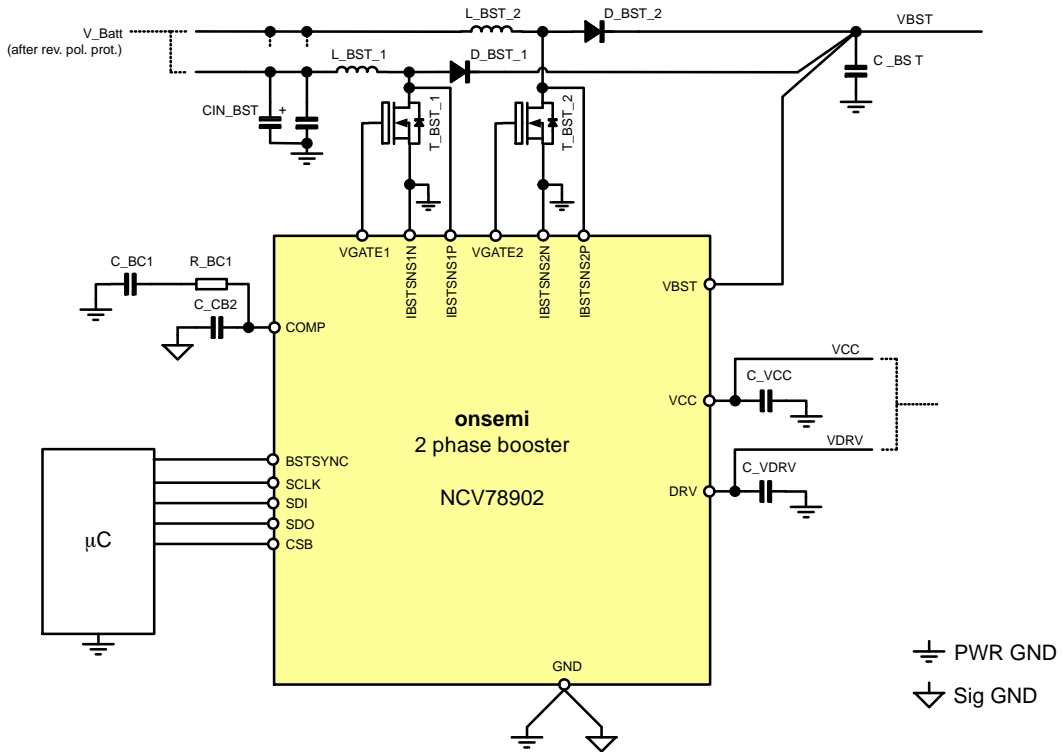
Figure 2. Typical Application Schematic – Current Sensing on Booster MOSFETs

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Figure 3. Typical Application Schematic SEPIC Configuration

Figure 4. Typical Application Schematic – SEPIC Configuration with Current Sensing on MOSFETs
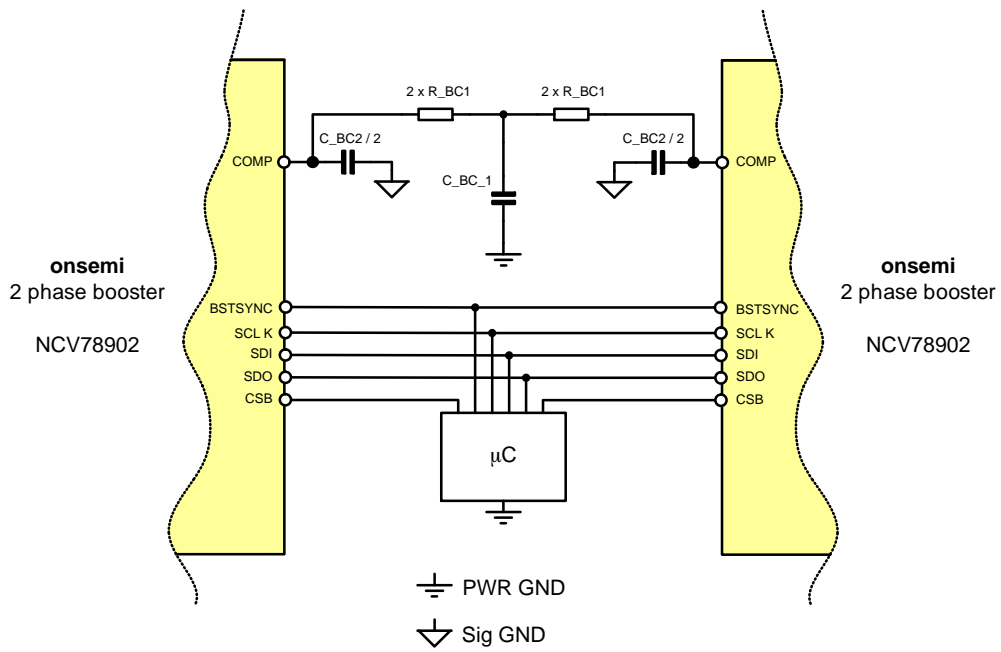
NCV78902

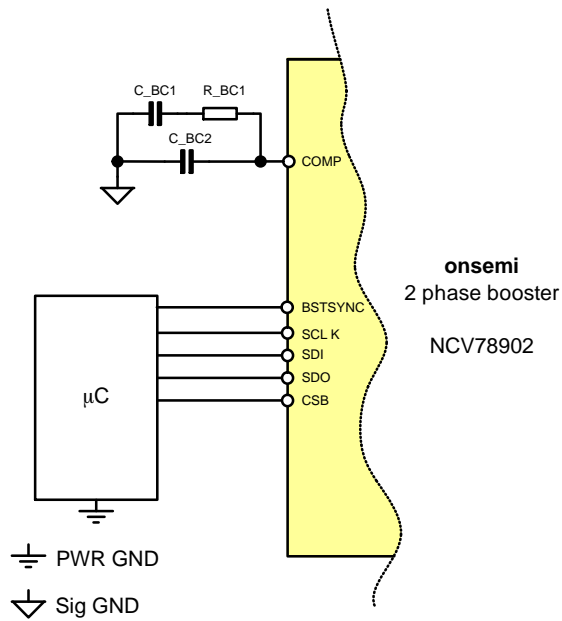**Figure 5. Application Schematic – COMP Connection when Using 4 Phase Booster**

Figure 6. Application Schematic – COMP Connection when Using 2 Phase Booster

NCV78902
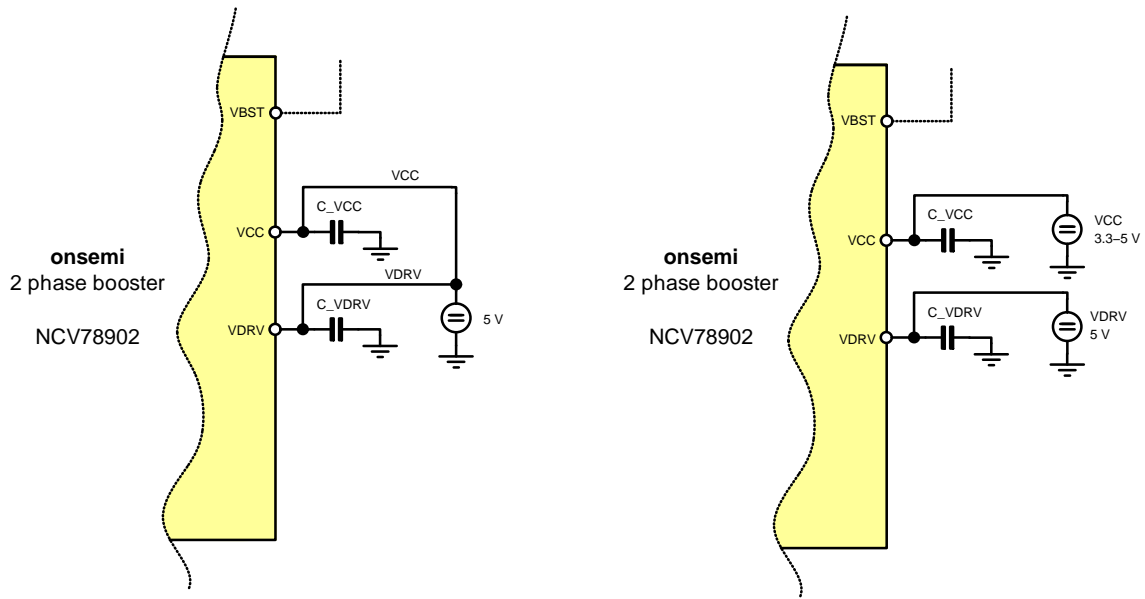
Figure 7. Application Schematic – SUPPLY Connection Possibilities

Table 1. EXTERNAL COMPONENTS

Component	Function	Typ. Value	Unit
C_VCC	V_{CC} Decoupling Capacitor	470	nF
C_DRV	V_{DRIVE} Decoupling Capacitor	470	nF
T_BST_x	Boost Regulator External Switch (Note 1)	NVMFS6H858NLWFT1G	
D_BST_x	Boost Regulator External Diode	NRVB10100MFST1G	
RSN_BST_x	Booster Shunt Resistor	10	mΩ
L_BST_x	Boost Regulator Inductor	10	μH
C_BST	Booster Ceramic Output Capacitor	22	μF
C_BST_E	Optional Booster Electrolytic Output Capacitor	22	μF
COMP	Booster Compensation Network Components	C_BC1 = 47 nF, R_BC1 = 3.3 kΩ, C_BC2 = 470 pF	

1. Logic level N-Channel MOSFET.

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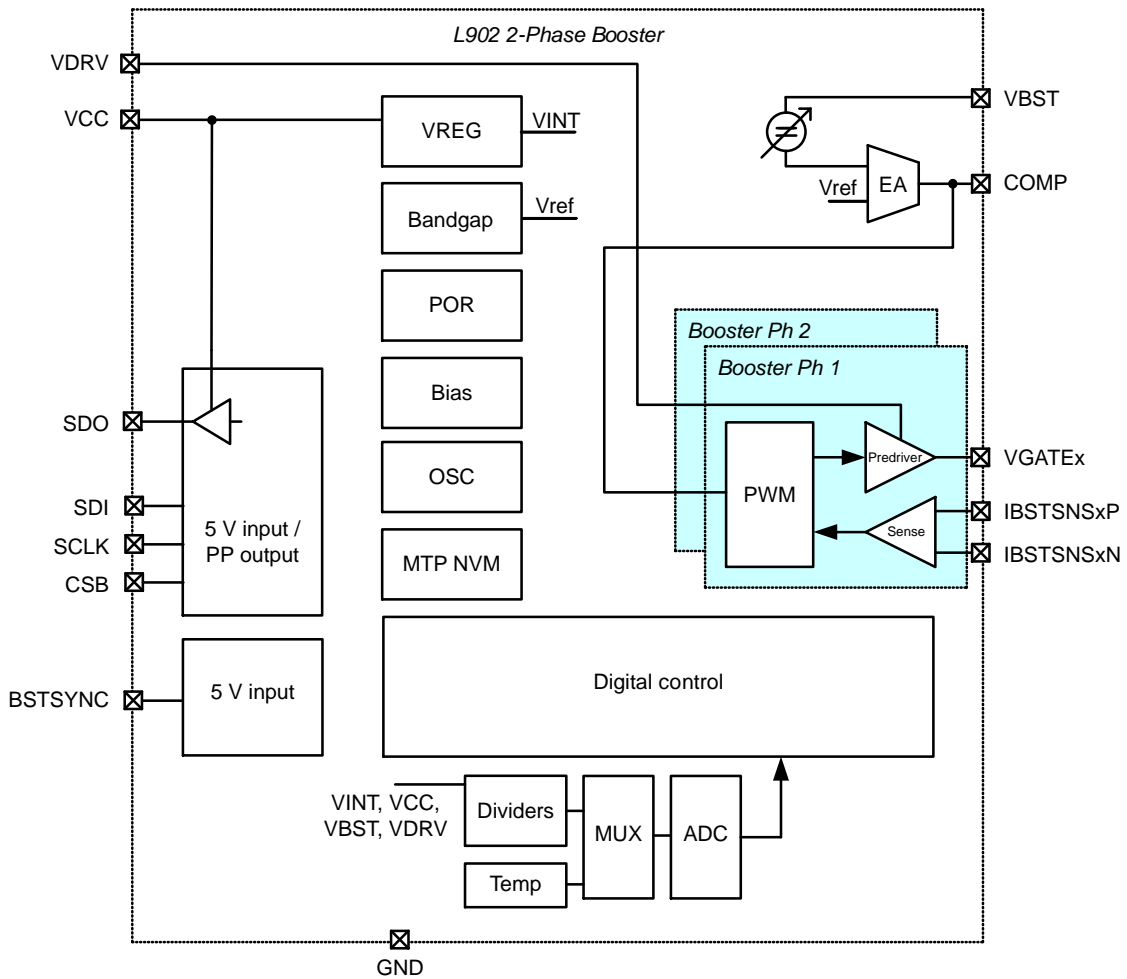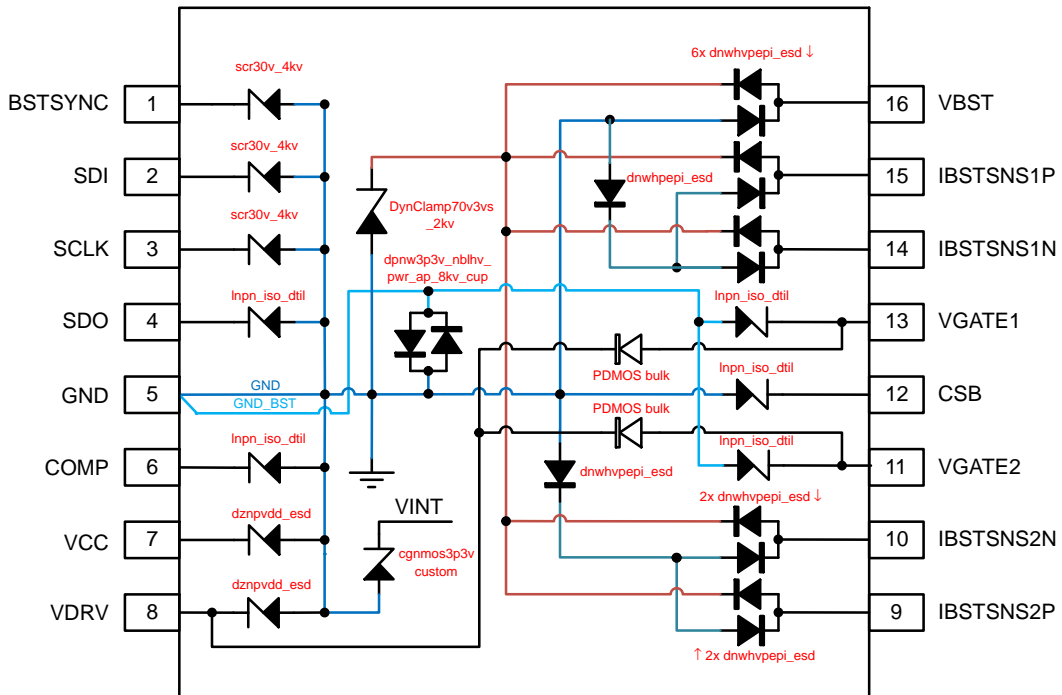**Figure 8. Block Diagram**

Figure 9. ESD Schematic

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PACKAGE AND PIN DESCRIPTION
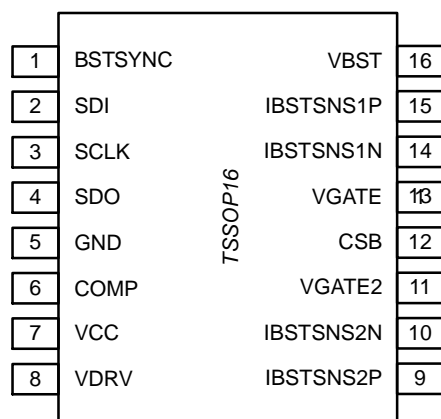
Figure 10. Pin Connections – TSSOP16 (Top View)

Table 2. PIN DESCRIPTION

Pin No.	Pin Name	Description	I/O Type
1	BSTSYNC	External clock for the booster	DI, 5V
2	SDI	SPI data in pin	DI, 5V
3	SCLK	SPI clock pin	DI, 5V
4	SDO	SPI data out pin	DO, 5V
5	GND	Ground	Ground
6	COMP	Compensation for the boost regulator	MV Analog
7	VCC	3.3 V/5 V voltage supply	MV Supply
8	VDRV	5 V voltage supply	MV Supply
9	IBSTSNS2P	Booster current positive feedback input (phase 2)	HV Analog
10	IBSTSNS2N	Booster current negative feedback input (phase 2)	HV Analog
11	VGATE2	Booster MOSFET gate pre-driver (phase 2)	MV Analog, DO
12	CSB	SPI chip select pin	DI, 5 V
13	VGATE1	Booster MOSFET gate pre-driver (phase 1)	MV Analog, DO
14	IBSTSNS1N	Booster current negative feedback input (phase 1)	HV Analog
15	IBSTSNS1P	Booster current positive feedback input (phase 1)	HV Analog
16	VBST	Booster voltage feedback input	HV Analog

Table 3. ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Min	Max	Unit
Ground Voltage	GND	0	0	V
Boost Voltage Feedback Input	VBST	−0.3	66 (Note 2)	V
VCC Supply Voltage	VCC	−0.3	6	V
VDRV Supply Voltage	VDRV	−0.3	6	V
SPI Clock Signal	SCLK	−0.3	6	V
SPI Chip Select Signal	CSB	−0.3	6	V
SPI Data Input Signal	SDI	−0.3	6	V
SPI Data Output Signal	SDO	−0.3	VCC + 0.3	V
BSTSYNC Signal	BSTSYNC	−0.3	6	V
Boost Current Sensing Positive Input	IBSTSNSxP	−1	68 (Note 2)	V
Boost Current Sensing Negative Input	IBSTSNSxN	−1	68 (Note 2)	V
Boost Regulator Stability Compensation	COMP	−0.3	6	V
Boost Switch Gate Driver Output	VGATE	−0.3	VDRV + 0.3	V
Storage Temperature (Note 3)	T_{STRG}	−50	150	°C
Electrostatic Discharge on Component Level Human Body Model (Note 4)	V_{ESD_HBM}	−2	+2	kV
Electrostatic Discharge on Component Level Charge Device Model (Note 4)	V_{ESD_CDM}	−500	+500	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. Absolute maximum rating for VBST and IBSTSNSxP pins is 70 V for limited time < 50 ms to comply with ISO21780:2020
3. For limited time up to 100 hours. Otherwise the max storage temperature is 85 °C.
4. This device series incorporates ESD protection and is tested by the following methods:
    ESD Human Body Model tested per ANSI/ESDA/JEDEC JS−001
    ESD Charge Device Model tested per EIA−JESD22−C101
    Latch-up Current Maximum Rating: ±100 mA per JEDEC standard: JESD78

Operating ranges define the limits for functional operation and parametric characteristics of the device. A mission profile (Note 5) is a substantial part of the operation conditions; hence the Customer must contact **onsemi** in order to mutually agree in writing on the allowed missions profile(s) in the application.

Table 4. RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
VCC Voltage Supply	VCC	3	3.3/5	5.5	V
VCC Voltage Supply during Memory Programming (Note 6)	VCCM	3.1	–	5.5	V
VDRV Supply Voltage	VDRV	4.5	5	5.5	V
IBSTSNSxN Operating Voltage Range	BST_VSNSN	−0.2	–	0.2	V
Ambient Temperature Range	T_A	−40	–	125	°C
Parametric Operating Junction Temperature Range (Note 7, 9)	T_{JP}	−40	–	145	°C
Functional Operating Junction Temperature Range (Note 8, 9)	T_{JF}	−45	–	150	°C
Junction Temperature Range during Memory Programming (Note 6, 9)	T_{JM}	−40	–	85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
5. A mission profile describes the application specific conditions such as, but not limited to, the cumulative operating conditions over life time, the system power dissipation, the system's environmental conditions, the thermal design of the customer's system, the modes, in which the device is operated by the customer, etc.
6. Memory programming limited to 100 cycles.
7. The parametric characteristics of the circuit are not guaranteed outside the Parametric operating junction temperature range.
8. The circuit functionality is not guaranteed outside the Functional operating junction temperature range. Also please note that the device is verified on bench for operation up to 170 °C.
9. Temperature reported by internal temperature sensor.

Table 5. THERMAL RESISTANCE

Characteristic	Package	Symbol	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient (Note 10)	TSSOP16	Rthja	–	175	–	°C/W

10. 4 layer PCB 50 x 50 x 1.5 mm, Cu layer thickness: Outer layers: 53 μm thickness, Inner layers: 35 μm thickness, Outer layers: 20% Cu coverage, Inner layers: 80% Cu coverage.

Table 6. ELECTRICAL CHARACTERISTICS (All Min and Max parameters are guaranteed over full junction temperature (T_{JP}) range (–40 °C; 145 °C), unless otherwise specified.)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
CURRENT CONSUMPTION						
The VCC Current Consumption	I_VCC		–	4	7	mA
Leakage Current in OFF State (Note 11)	ILEAK_OFF	VCC = 0 V, VBST, IBSTSNSxP = 16 V, SDI, SCLK, CSB, BSTSYNC = 5 V Temperature range: –40 °C to 85 °C	–	–	10	μA
OSC16M: SYSTEM OSCILLATOR CLOCK						
Oscillator Output Frequency (Trimmed)	OSC_CLK	OSC_CAL[4:0] = 0	14.8	16	17.2	MHz
Oscillator Output Frequency (Untrimmed)	OSC_CLK_0	OSC_CAL[4:0] = 0, TRIMERR = 1	6	11	20	MHz
Oscillator Frequency Calibration Step	OSC_SCAL	Trimmed oscillator. Calibrated via OSC_CAL[4:0] SPI register	40	100	160	kHz
Oscillator Duty Cycle	OSC_DUTY		40	50	60	%
VINT: 3 V LOW VOLTAGE INTERNAL ANALOG AND DIGITAL SUPPLY						
The VINT Voltage @ VCC = 5.5 V	VINT_VCC5	Iload = 0 to 10 mA	3	3.15	3.4	V
The VINT Voltage @ VCC = 3.0 V	VINT_VCC3	Iload = 5 mA	2.8	–	–	V
VINT POR Threshold, VINT Rising	POR_R		2.5	2.6	2.7	V
VINT POR Threshold, VINT Falling	POR_F		2.4	–	2.6	V
VINT POR Hysteresis	POR_H		–	0.05	–	V
The POR Debounce Time (Both Edges)	POR_DEB		0.5	2	6	μs
VDRIVE: SUPPLY FOR BOOSTER MOSFET GATE DRIVE CIRCUIT AND BUCK LOW SIDE SWITCHES						
VDRV UV Detection Threshold	VDRV_UV7	VDRV_UV_THR[2:0] = 111	4.2	4.4	4.6	V
	VDRV_UV6	VDRV_UV_THR[2:0] = 110	3.9	4.1	4.3	V
	VDRV_UV5	VDRV_UV_THR[2:0] = 101	3.6	3.8	4.0	V
	VDRV_UV4	VDRV_UV_THR[2:0] = 100	3.3	3.5	3.7	V
	VDRV_UV3	VDRV_UV_THR[2:0] = 011	3.0	3.2	3.4	V
	VDRV_UV2	VDRV_UV_THR[2:0] = 010	2.8	2.9	3.0	V
	VDRV_UV1	VDRV_UV_THR[2:0] = 001	2.5	2.6	2.7	V
VDRV UV Detection Threshold Disabled	VDRV_UV0	VDRV_UV_THR[2:0] = 000	–	0	–	V
VDRV UV Detection Release Threshold	VDRV_NOUV7	VDRV_UV_THR[2:0] = 111	4.3	4.5	4.7	V
	VDRV_NOUV6	VDRV_UV_THR[2:0] = 110	3.95	4.2	4.4	V
	VDRV_NOUV5	VDRV_UV_THR[2:0] = 101	3.65	3.9	4.1	V
	VDRV_NOUV4	VDRV_UV_THR[2:0] = 100	3.25	3.6	3.8	V
	VDRV_NOUV3	VDRV_UV_THR[2:0] = 011	3.05	3.3	3.5	V
	VDRV_NOUV2	VDRV_UV_THR[2:0] = 010	2.85	3.0	3.1	V
	VDRV_NOUV1	VDRV_UV_THR[2:0] = 001	2.55	2.7	2.8	V

Table 6. ELECTRICAL CHARACTERISTICS (All Min and Max parameters are guaranteed over full junction temperature (T_{JP}) range (–40 °C; 145 °C), unless otherwise specified.) (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDRIVE: SUPPLY FOR BOOSTER MOSFET GATE DRIVE CIRCUIT AND BUCK LOW SIDE SWITCHES						
VDRV UV Voltage Threshold Hysteresis	VDRV_UVHyst		50	–	200	mV
VDRV UV Propagation Delay without Debouncer	VDRV_UVDLNODB		–	–	200	ns
VDRV UV Detection Delay	VDRV_UVDL	Debouncer at falling edge of VDRV voltage	–	8	–	µs
ADC FOR MEASURING VBST, VCC, VDRV, VINT, TEMP						
ADC Resolution	ADC_RES		–	9	–	Bits
Integral Nonlinearity (INL)	ADC_INL	Best fitting straight line method. Between 5% and 95% of input full scale voltage.	–2	–	2	LSB
Differential Nonlinearity (DNL)	ADC_DNL	Best fitting straight line method. Between 5% and 95% of input full scale voltage.	–2	–	2	LSB
ADC Offset at Output	ADC_OFFS		–5	–	5	LSB
ADC Gain Error at Output	ADC_GAIN_ERR	Best fitting straight line method. Between 5% and 95% of input full scale voltage.	–5	–	5	%
Time for 1 SAR Conversion	ADC_CONV		–	7.5	–	µs
ADC Full Scale for VBST Measurement	ADC_VBST		66.5	70	73.5	V
ADC Full Scale for VCC Measurement	ADC_VCC		5.86	6.18	6.5	V
ADC Full Scale for VDRV Measurement	ADC_VDRV		5.86	6.18	6.5	V
ADC Full Scale for VINT Measurement	ADC_VINT		4.6	4.8	5	V
Temperature Measurement Range	TMP_RG	Typical values	–60	–	195	°C
Temperature Measurement Resolution	TMP_RES	Typical values	–	1.05	–	°C/LSB
TSD Threshold Level (VTEMP[8:0] = 410)	TSD	Guaranteed by trimming	160	170	180	°C
BOOST CONTROLLER – VOLTAGE REGULATION PARAMETERS						
Booster Overvoltage Shutdown ΔV to the Reg. Level (Note 12)	BST_OV7	BST_OV_SD[2:0] = 111	5.3	5.7	6.3	V
	BST_OV6	BST_OV_SD[2:0] = 110	4.3	4.8	5.3	V
	BST_OV5	BST_OV_SD[2:0] = 101	3.5	3.9	4.3	V
	BST_OV4	BST_OV_SD[2:0] = 100	2.7	3	3.3	V
	BST_OV3	BST_OV_SD[2:0] = 011	2.2	2.5	2.8	V
	BST_OV2	BST_OV_SD[2:0] = 010	1.7	2	2.3	V
	BST_OV1	BST_OV_SD[2:0] = 001	1.2	1.5	1.8	V
	BST_OV0	BST_OV_SD[2:0] = 000	0.8	1	1.2	V
Booster Overvoltage Re-activation	BST_RA3	BST_OV_REACT[1:0] = 11	–1.9	–1.5	–1.1	V
	BST_RA2	BST_OV_REACT[1:0] = 10	–1.3	–1.0	–0.7	V
	BST_RA1	BST_OV_REACT[1:0] = 01	–0.65	–0.5	–0.35	V
	BST_RA0	BST_OV_REACT[1:0] = 00	–	0	–	V

Table 6. ELECTRICAL CHARACTERISTICS (All Min and Max parameters are guaranteed over full junction temperature (T_{JP}) range (–40 °C; 145 °C), unless otherwise specified.) (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOOST CONTROLLER – VOLTAGE REGULATION PARAMETERS						
Booster Voltage Feedback Fail Detection Threshold	BST_FBFAIL		1.15	1.21	1.27	V
Booster Regulation Level	BST_REG_127		–	62	–	V
	BST_REG_000		–	9.7	–	V
Booster Regulation Level Increase per Code	ΔBST_REG	Linear increase, 7 bits	–	0.412	–	V
Booster Regulation Level Error	BST_REGERRH	VBST_NOM > 25 V	–3	–	3	%
	BST_REGERRL	VBST_NOM < 25 V	–4	–	4	%
Booster Error Amplifier (EA) Trans-conductance Gain G_m Seen from VBST	EA_GM3	VBST = VBST_REG ±1 V 0.5 V < VCOMP < 2.1 V BST_OTA_GAIN[1:0] = 11	42	60	78	μS
	EA_GM2	BST_OTA_GAIN[1:0] = 10	21	30	39	μS
	EA_GM1	BST_OTA_GAIN[1:0] = 01	10	15	20	μS
Error Amplifier High Impedance State	EA_GM0	BST_OTA_GAIN[1:0] = 00	–	0	–	μS
EA Max Output Current (Positive/ Sink)	EA_IOUT3P	BST_OTA_GAIN[1:0] = 11	100	130	160	μA
	EA_IOUT2P	BST_OTA_GAIN[1:0] = 10	50	65	80	μA
	EA_IOUT1P	BST_OTA_GAIN[1:0] = 01	25	32.5	40	μA
EA Min Output Current (Negative/ Source)	EA_IOUTN		–900	–530	–300	μA
EA Equivalent Output Resistance	EA_BLR	VCOMP = 0.5 V	0.8	2.4	4.6	MΩ
EA Max Output Leakage Current in Hi Impedance State	EA_BLI_P	VCC present, VCOMP = 2.1 V	0.15	0.4	1	μA
	EA_BLI	VCC = 0 V, VCOMP = 2.1 V	0.5	1.7	5	μA
COMP Short Circuit Current	EA_INLIM	BST_OTA_GAIN[1:0] = 11 VBST = 55 V, VCOMP = 0 V	–1.5	–	–	mA
EA Low Clamp Voltage	COMP_CLL		–	–	0.45	V
EA Low Clamp Current Limitation	COMP_CLL_ILIM		–0.5	–	–0.1	mA
EA High Clamp Offset Voltage	COMP_CLH	Current limitation mode	60	–	320	mV
Booster Skip Cycle for Low Currents (Booster Disabled for Lower VCOMP)	BST_SKCL0	BST_SKCL[1:0] = 00	0.50	0.55	0.60	V
	BST_SKCL1	BST_SKCL[1:0] = 01	0.56	0.6	0.64	V
	BST_SKCL2	BST_SKCL[1:0] = 10	0.66	0.7	0.75	V
	BST_SKCL3	BST_SKCL[1:0] = 11	0.75	0.8	0.85	V
Accuracy of Timer for BST_TOFF_MIN and BST_TON_MIN	BST_OSC_ERR		–15	–	15	%
BOOST CONTROLLER – CURRENT REGULATION PARAMETERS						
COMP Buffer Offset	BST_CBUF_OFFS		–20	–	20	mV
COMP Buffer Step	BST_CBUF_STEP		6	10	14	mV

Table 6. ELECTRICAL CHARACTERISTICS (All Min and Max parameters are guaranteed over full junction temperature (T$_{JP}$) range (−40 °C; 145 °C), unless otherwise specified.) (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOOST CONTROLLER – CURRENT REGULATION PARAMETERS						
Division Factor of VCOMP Voltage Towards the Current Comparator Input	COMP_DIV0	BST_COMP_DIV[2:0] = 000	1.88	2	2.12	
	COMP_DIV1	BST_COMP_DIV[2:0] = 001	2.69	2.8	2.91	
	COMP_DIV2	BST_COMP_DIV[2:0] = 010	3.84	4	4.16	
	COMP_DIV3	BST_COMP_DIV[2:0] = 011	5.47	5.7	5.93	
	COMP_DIV4	BST_COMP_DIV[2:0] = 100	7.68	8	8.32	
	COMP_DIV5	BST_COMP_DIV[2:0] = 101	10.85	11.3	11.75	
	COMP_DIV6	BST_COMP_DIV[2:0] = 110	15.36	16	16.64	
	COMP_DIV7	BST_COMP_DIV[2:0] = 111	21.69	22.6	23.52	
Voltage Shift (Offset) on VCOMP on Current Comparator Input	COMP_VSF		0.455	0.5	0.545	V
Current Comparator for Imax Detection	BST_VLIMTH255	BST_VLIM_THR[7:0] = 11111111	570	600	630	mV
	BST_VLIMTH0	BST_VLIM_THR[7:0] = 00000000	−3	2	7	mV
Imax Detection Increase per Code	ΔBST_VLIMTH	Linear increase, 8 bits	−	2.35	−	mV
Current Comparator for Imax Detection Error	BST_VLIMTHERR		−5 & −5	−	5 & 5	% & mV
Current Regulation Comparator Offset Voltage	BST_OFFS		−5	−	5	mV
Booster Slope Compensation	BST_SLCTR7	BST_SLP_CTRL[2:0] = 111	1065	1210	1355	mV/μs
	BST_SLCTR6	BST_SLP_CTRL[2:0] = 110	695	790	885	mV/μs
	BST_SLCTR5	BST_SLP_CTRL[2:0] = 101	430	500	570	mV/μs
	BST_SLCTR4	BST_SLP_CTRL[2:0] = 100	306	360	414	mV/μs
	BST_SLCTR3	BST_SLP_CTRL[2:0] = 011	187	220	253	mV/μs
	BST_SLCTR2	BST_SLP_CTRL[2:0] = 010	120	150	180	mV/μs
	BST_SLCTR1	BST_SLP_CTRL[2:0] = 001	57	75	93	mV/μs
	BST_SLCTR0	BST_SLP_CTRL[2:0] = 000	−	0	−	mV/μs
BOOST CONTROLLER – MOSFET GATE DRIVER						
High-side Switch Impedance	FETDRV_RONH		−	4	7	Ω
Low-side Switch Impedance	FETDRV_RONL		−	4	7	Ω
Pull-down Resistor	FETDRV_RPD		4	10	18	kΩ
5 V TOLERANT DIGITAL INPUTS (SCLK, CSB, SDI, BSTSYNC)						
High Level Input Voltage	DI5_VINH	VINT = 2.7 V to 3.6 V	2	−	−	V
Low Level Input Voltage	DI5_VINL	VINT = 2.7 V to 3.6 V	−	−	0.8	V
Input Threshold Hysteresis	DI5_VINHyst		100		900	mV
The Pull-up/down Resistance (Note 13)	DI5_RP		40	100	180	kΩ
Input Leakage Current	DI5_ILIN	Pull resistance disabled	−1	−	1	μA
5 V DIGITAL OUTPUT (SDO)						
High Level Output Voltage	DO5_VOH	Iout = −2 mA (current flows into the pin)	VCC − 0.5	−	VCC	V
Low Level Output Voltage	DO5_VOL	Iout = 2 mA	0	−	0.5	V
Output Delay; Both Edges	DO5_DEL	Cload = 50 pF	−	7	30	ns

Table 6. ELECTRICAL CHARACTERISTICS (All Min and Max parameters are guaranteed over full junction temperature (T$_{JP}$) range (–40 °C; 145 °C), unless otherwise specified.) (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SPI INTERFACE						
CSB Setup Time	csb_setup	CSB setup time before first SCLK rising edge	375	–	–	ns
CSB Hold Time	csb_hold	CSB hold time after last SCLK rising edge	150	–	–	ns
CSB High Time	csb_gap	Gap between two CSB low pulses	500	–	–	ns
SCLK Clock Period	sclk_per		250	–	–	ns
SCLK Low Time	sclk_lo		0.4 x sclk_per	–	0.6 x sclk_per	ns
SCLK High Time	sclk_hi		0.4 x sclk_per	–	0.6 x sclk_per	ns
SDI Setup Time before Each SCLK Rising Edge	sdi_setup		45	–	–	ns
SDI Hold Time after Each SCLK Rising Edge	sdi_hold		45	–	–	ns
SDO Hold Time	sdo_hold	Depends on parasitic capacitance of SDO line	0	–	62.5 + Max (DO5_DEL)	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

11. Sum of currents from, VBST, IBSTSNSxP, SDI, SCLK, CSB, and BSTSYNC pin.
12. User has to take care that sum of selected Booster regulation level BST_REG and Booster overvoltage shutdown BST_OV including accuracy and overshoots does not to exceed Absolute Maximum ratings 66 V for Buck Input voltage VINx and Boost voltage feedback input VBST.
13. Pull-down resistance for SCLK, SDI, BSTSYNC; pull-up resistance to VINT for CSB.
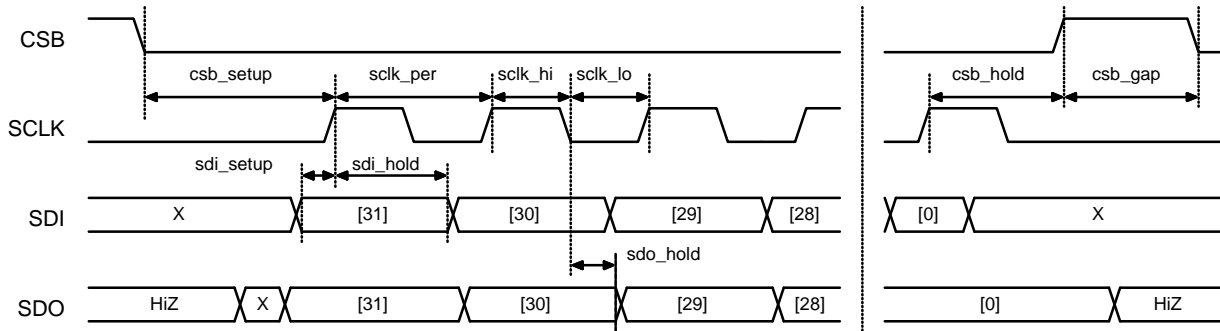

Figure 11. SPI Communication Timing

DETAILED OPERATING DESCRIPTION

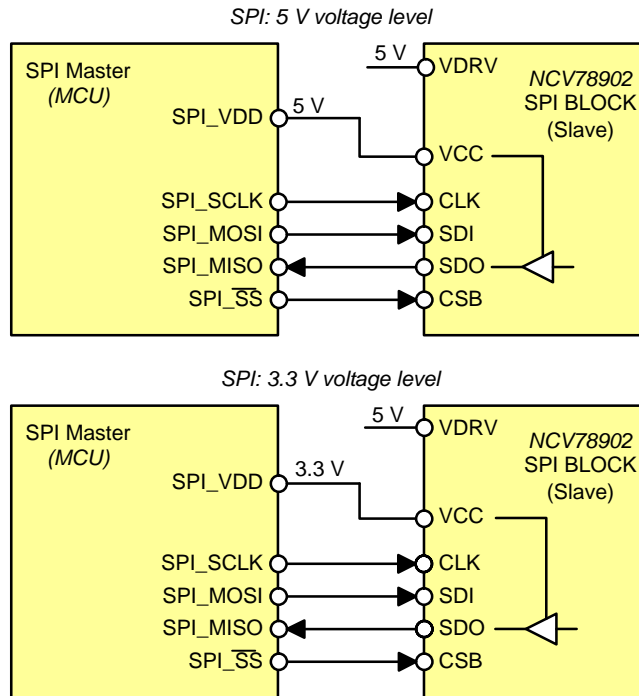*SPI: 5 V voltage level*

SPI: 3.3 V voltage level

Figure 12. SPI Connection Scenarios and Power Supply Strategy

SUPPLY CONCEPT IN GENERAL

Only two low voltage supplies have to be brought to the NCV78902 chip – VCC and VDRV supply. More detailed description follows.

VDRV Supply

The VDRV supply voltage represents the power for booster pre-driver block which generates the VGATE, used to switch external booster MOSFET. This supply is separated from the VCC to limit the noise on sensitive circuitries. 5 V is required for reliable operation over wide operating conditions.

VDRV Undervoltage Lockout safety mechanism monitors sufficient voltage for booster MOSFETs and protects them by switching off the booster when VDRV voltage is too low. Detection level is set by VDRV_UV_THR[2:0] register (see Table 6 – VDRIVE: SUPPLY FOR BOOSTER MOSFET GATE DRIVE CIRCUIT AND BUCK LOW SIDE SWITCHES section for more details). When VDRV_UV_THR[2:0] = 0, the function is disabled. VDRV_UV (latched, reg. 0x36) flag indicates that protection has acted.

VCC Supply

The VCC supply voltage represents power for the internal supply VINT. It also defines interface voltage with the microcontroller on push-pull SDO pin and shall be selected accordingly (3.3 or 5 V).

By disconnecting the VCC supply, the Low power mode can be entered. In typically setup small external switch can be placed into VCC supply line.

VINT Supply

The internal regulator generates the main low voltage digital and analog supply VINT for the chip.

The Power-On-Reset circuit (POR) monitors the VINT voltage to control the out-of-reset and reset entering state. At power-up, the chip will exit from reset state when VINT > POR_R. No SPI communication is possible in reset state.

Internal Clock Generation

An internal RC clock generator is used to run all the digital functions in the chip. The clock is trimmed in the factory prior to delivery. Its accuracy is guaranteed under full operating conditions and is independent from external component selection. All timings depend on OSC_CLK accuracy (refer to Table 6 – OSC16M: SYSTEM OSCILLATOR CLOCK section for details).

In the application, the oscillator can be further calibrated via OSC_CAL[4:0] SPI register.

For this purpose the CSB_DUR[19:0] register is introduced, which allows to measure duration of CSB signal, precisely generated by MCU, and by this way indirectly check the oscillator frequency.

ADC

General

The built-in analog to digital converter (ADC) is an 9-bit capacitor based successive approximation register (SAR). This embedded peripheral can be used to provide the following measurements to the external Micro Controller Unit (MCU):

- VDRV voltage: sampled at the VDRV pin;
- VCC voltage: sampled at the VCC pin;
- VINT voltage;
- VBST booster voltage: sampled at VBST pin;
- VTEMP measurement (chip temperature);

The internal NCV78902 ADC state machine samples all the above channels automatically, taking care for setting the analog MUX and storing the converted values in memory. The external MCU can readout all ADC measured values via the SPI interface, in order to take application specific decisions. Please note that none of the MCU SPI commands interfere with the internal ADC state machine sample and conversion operations: the MCU will always get the last available data at the moment of the register read.

Basic measurement cycle consists from the measurements in shown order:

$$VTEMP \rightarrow VINT \rightarrow VCC \rightarrow VDRV \rightarrow VBST$$

Supply Voltage ADC: V_{CC}

The supply voltage is sampled at VCC pin. The (9-bit) conversion ratio is 6.18/511 (V/dec) = 12.3 (mV/dec) typical. The converted value can be found in the SPI register VCC[8:0].

Supply Voltage ADC: V_{DRV}

The supply voltage is sampled at VDRV pin. The (9-bit) conversion ratio is 6.18/511 (V/dec) = 12.3 (mV/dec) typical. The converted value can be found in the SPI register VDRV[8:0].

Logic Supply Voltage ADC: V_{INT}

The logic supply voltage is sampled internaly. The (9-bit) conversion ratio is 4.8/511 (V/dec) = 9.4 (mV/dec) typical. The converted value can be found in the SPI register VINT[8:0].

Booster Voltage ADC: V_{BST}

The booster voltage is sampled at VBST pin. The (9-bit) conversion ratio is 70/511 (V/dec) = 0.137 (V/dec) typical. The converted value can be found in the SPI register VBST[8:0]. There is internal RC filter consisting of 10 MΩ and 5 pF on VBST pin filtering out the booster voltage ripple. This measurement can be used by the MCU for diagnostics and booster control loop monitoring.

Device Temperature ADC: V_{TEMP}

By means of the VTEMP measurement, the MCU can monitor the device junction temperature (T_J) over time. The conversion formula is:

$$T_J = 1.05 \cdot (VTEMP[8:0] - 248) \qquad \text{(eq. 1)}$$

VTEMP[8:0] is the value read out directly from the related SPI register. The value is also used internally by the device for the *thermal warning* and *thermal shutdown* functions. More details on these diagnostic flags can be found in the dedicated sections in this document.

BOOSTER REGULATOR

General

The NCV78902 features two-phase booster stage which provides the required voltage source for the LED string voltages out of the available battery voltage. Moreover, it filters out the variations in the battery input current in case of LED strings PWM dimming.

For nominal loads, the boost controller will regulate in *continuous* mode of operation, thus maximizing the system power efficiency at the same time having the lowest possible input ripple current (with "continuous mode" it is meant that the supply current does not go to zero while the load is activated). Only in case of very low loads or low dimming duty cycle values, *discontinuous* mode can occur: this means the supply current can swing from zero when the load is off, to the required peak value when the load is on, while keeping the required input average current through the cycle. In such situations, the total efficiency ratio may be lower than the theoretical optimal. However, as also the total losses will at the same time be lower, there will be no impact on the thermal design.

The booster can be operated in *multi-phase* mode by combining more NCV78902 devices in the application. More details about the multiphase mode can be found in the dedicated section.

Booster Regulation Principles

The NCV78902 features *current-mode* voltage controller, which regulates the VBST line used by the buck converters. The regulation loop principle is shown in the following picture. The loop compares the reference voltage (BST_VSETPOINT[6:0]) with the actual measured voltage at the VBST pin, thus generating an error signal which is treated internally by the error trans-conductance amplifier (block A1). This amplifier transforms the error voltage into current by means of the trans-conductance gain Gm. The amplifier's output current is then fed into the external compensation network impedance (A2), so that it originates a voltage at the COMP pin, this last used as a reference by the current control block (B).

The current controller regulates the duty cycle as a consequence of the COMP reference, the sensed inductor peak current via the external resistor RSENSE and the slope compensation used. The power converter (block C) represents the circuit formed by the boost converter externals (inductor, capacitors, MOSFET and forward diode). The load power (usually the LED power going via the buck converters) is applied to the converter. The

controlled variable is the boost voltage, measured directly at the device VBST pin with a unity gain feedback (block F). The picture highlights as block G all the elements contained

inside the device. The regulation parameters are flexibly set by a series of SPI commands. A detailed internal boost controller block diagram is presented in the next section.
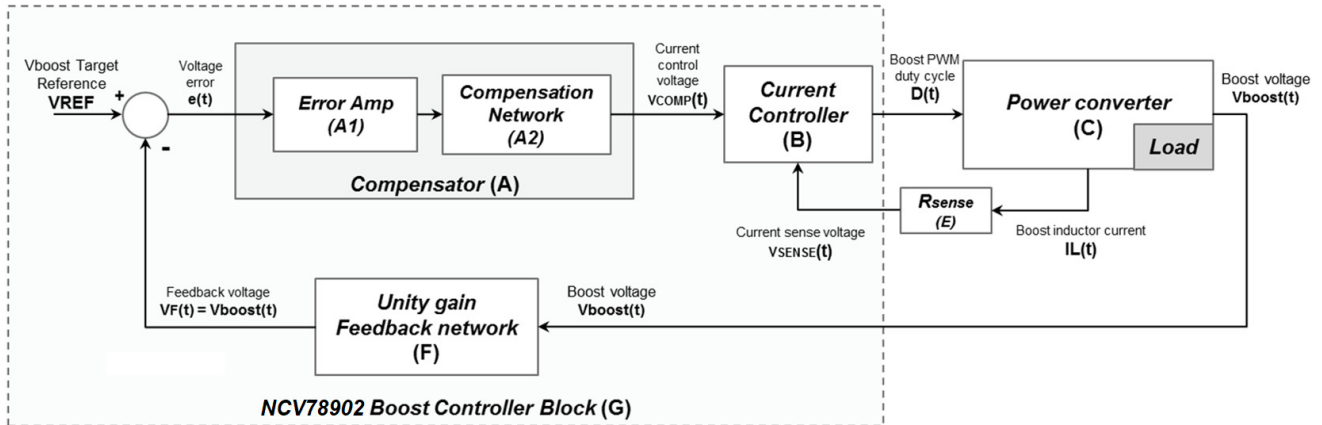

Figure 13. NCV78902 Boost Control Loop – Principle Block Diagram

Boost Controller Detailed Internal Block Diagram

A detailed NCV78902 boost controller block diagram is provided in this section. The main signals involved are indicated, with a particular highlight on the SPI programmable parameters.

The blocks referring to the principle block diagram are also indicated. In addition, the protection specific blocks can be found (see dedicated sections for details).
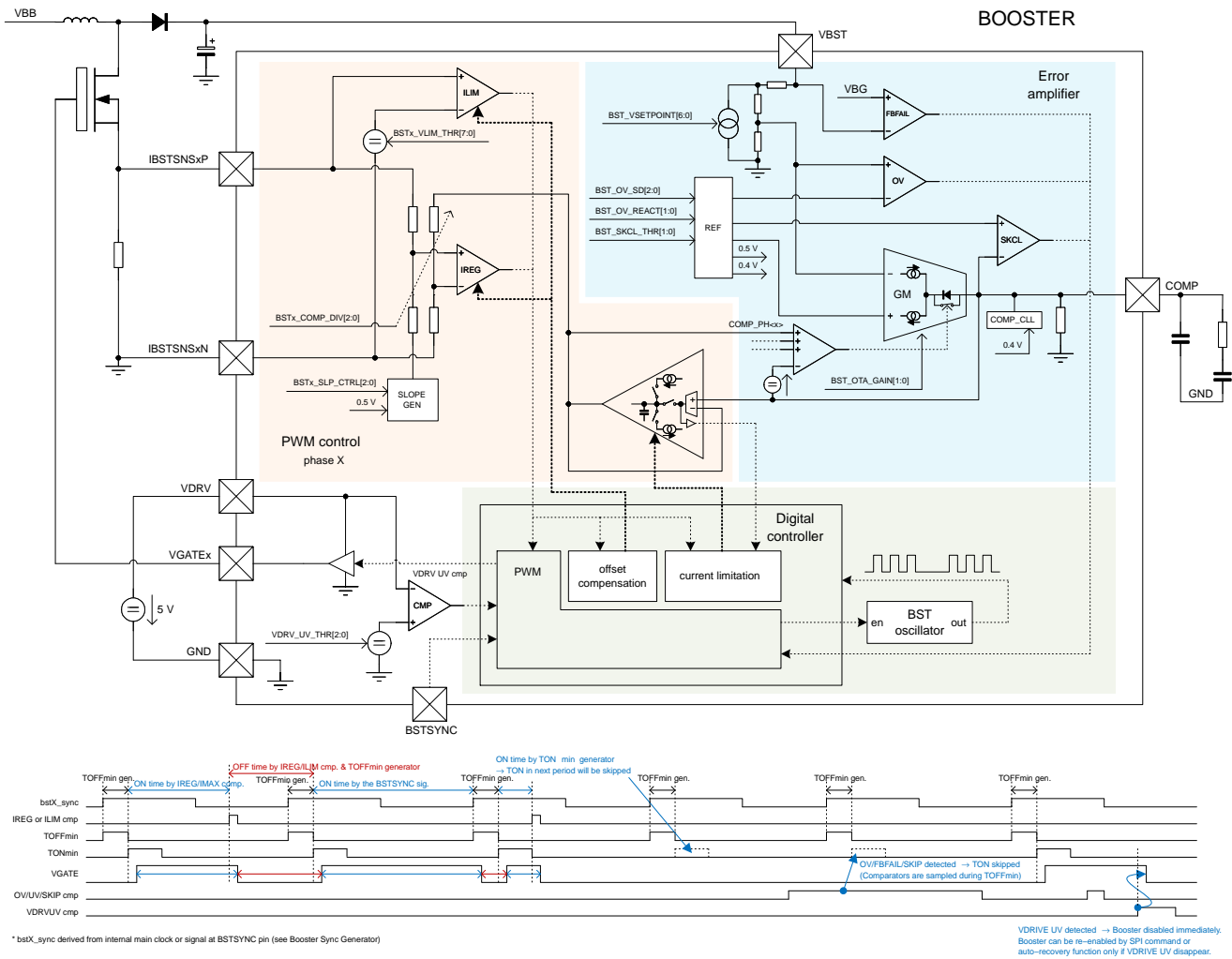
Figure 14. Boost Controller Internal Block Diagram

Booster Regulator Setpoint (BST_VSETPOINT)

The booster voltage VBST is regulated around the target programmable by the 7-bit SPI setting BST_VSETPOINT[6:0], ranging from a minimum of 9.7 V to a maximum of typical 62 V (please refer to Table 6 – BOOST CONTROLLER – VOLTAGE REGULATION PARAMETERS section for details) according to the following equation:

$$V_{BST\_NOM} = 9.7 + BST\_VSETPOINT[6:0] \times \left(\frac{52.3}{127}\right) [V]_{(eq.\ 2)}$$

Due to the step-up only characteristic of any boost converter, the boost voltage cannot obviously be lower than the supply battery voltage provided. Therefore a target of 9.7 V would be used only for systems that require the activation of the booster in case of battery drops below the nominal level. At power-up, the booster is disabled and the setpoint is per default the minimum (all zeroes).

Booster Overvoltage Shutdown Protection

An integrated comparator monitors VBST in order to protect the external booster components from overvoltage. When the voltage rises above the threshold defined by the sum of the booster voltage setpoint (BST_VSETPOINT[6:0]) and the overvoltage shutdown value (BST_OV_SD[2:0]), the MOSFET gate is switched-off at least for the current PWM cycle and at the same time, the boost overvoltage flag in the status register will be set (BST_OV = '1'), together with the BSTx_RUNNING flags equal to zero. The PWM runs again as from the moment the VBST will fall below the reactivation hysteresis defined by the BST_OV_REACT[1:0] SPI parameter. Therefore, depending on the voltage drop and the PWM frequency, it might be that more than one cycle will be skipped. A graphical interpretation of the protection levels is given in the Figure 15.

User has to take care that sum of selected Booster regulation level BST_REG and Booster overvoltage shutdown BST_OV including accuracy and overshoots does not to exceed Absolute Maximum ratings 66 V for Buck Input voltage VINx and Boost voltage feedback input VBST. For highest settings of Booster regulation level BST_REG, the lowest settings of Booster overvoltage shutdown threshold BST_OV should be selected.
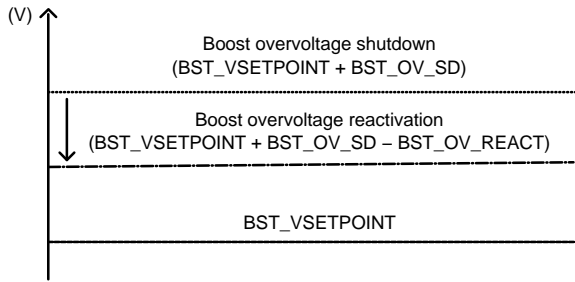
Figure 15. Booster Voltage Protection Levels with Respect to the Setpoint

After POR, the BST_OV flag may be set at first read out. Please note that the booster overvoltage detection is also active when Booster is OFF (booster disabled by SPI related bit). Please note that the tolerances of the booster setpoint level and the booster overvoltage and reactivation are given in Table 6 – BOOST CONTROLLER – VOLTAGE REGULATION PARAMETERS section.

Booster Current Regulation Loop

The peak-current level of the booster is set by the voltage of the compensation pin COMP, which is output of the trans-conductance error amplifier, "block B" of Figure 13. This reference voltage is fed to the current comparator via a divider (divider ratio of which can be set by register BSTx_COMP_DIV[2:0] for each phase independently, see Table 6 – BOOST CONTROLLER – CURRENT REGULATION PARAMETERS section for more details). The comparator compares this reference voltage with voltage VSENSE sensed on the external sense resistor RSENSE or over the booster MOSFET, connected to the pins IBSTSNSxP and IBSTSNSxN. The sense voltage is created by the booster inductor coil current when the MOSFET is switched on and is summed up to an additional offset of +0.5 V (see COMP_VSF in Table 6 – BOOST CONTROLLER – CURRENT REGULATION PARAMETERS section) and on top of that, a slope compensation voltage ramp is added. The slope compensation is programmable by SPI via the BSTx_SLP_CTRL[2:0] register for each phase independently and can also be disabled. Due to the offset, current can start flowing in the circuit when VCOMP > COMP_VSF.

When booster is active, voltage at COMP pin is clamped from bottom side to 0.45 V (see Table 6 – BOOST CONTROLLER – VOLTAGE REGULATION PARAMETERS section), from the top side no clamp is present and internally there is a circuitry with functionality ensuring quick recovery and fast reaction of the system to load changes. Working range of the COMP pin is from 0.5 V to 2.1 V.
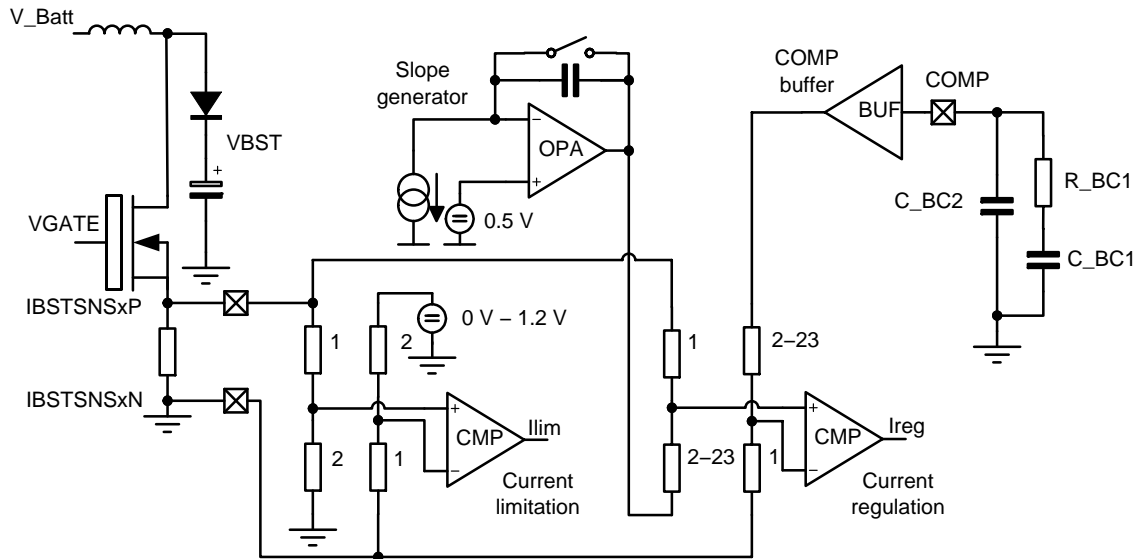

Figure 16. Booster Peak Current Regulator Involved in the Current Control Loop

Booster Current Limitation Protection

On top of the normal current regulation loop comparator, an additional comparator clamps the maximum physical current that can flow in the booster input circuit while the MOSFET is driven. The aim is to protect all the external components involved (boost inductor from saturation, boost diode and boost MOSFET from overcurrent, etc...). The protection is active PWM cycle-by-cycle and switches off the MOSFET gate when VSENSE reaches its maximum threshold defined by the BSTx_VLIM_THR[7:0] register (see Table 6 – BOOST CONTROLLER – CURRENT REGULATION PARAMETERS section for more details). Therefore, the maximum allowed peak current will be defined by the ratio

IPEAK_MAX = V(BSTx_VLIM_THR[7:0])/RSENSE or in case of sensing over booster MOSFET IPEAK_MAX = V(BSTx_VLIM_THR[7:0])/RDSon.

The maximum current must be set in order to allow the total desired booster power for the lowest battery voltage. Warning: setting the current limit too low may generate unwanted system behavior as uncontrolled de-rating of the LED light due to insufficient power.

Current limitation mode is mostly stable operating mode without subharmonic oscillations what allows to deliver maximum power to the load. Stable operation is achieved by regulating and tracking current limit threshold by dedicated algorithm. When booster phase regulates in this mode, ripple corresponding to regulation step BST_CBUF_STEP can be observed at inductor peak current. In certain border conditions some instabilities can occur, in such situation programming of longer PWM minimum on–time (BST_MIN_TON[1:0]) can help.

Booster PWM Internal Generation

This mode activated by BST_SRC = 1, creates the PWM frequency starting from the internal clock FOSC16M. A fine selection of frequencies is enabled by the register BST_SRC_FREQ[4:0], ranging from typical 125 kHz to typical 4 MHz (Table 6 – BOOST CONTROLLER – VOLTAGE REGULATION PARAMETERS section).

Maximum frequency per booster phase is supposed to be 2 MHz, so for example internally generated 4 MHz should be split to half between two phases.

Table 7. INTERNAL BOOSTER FREQUENCIES

BST_SRC_ FREQ[4:0]	Freq (kHz)	BST_SRC_ FREQ[4:0]	Freq (kHz)
0	125	16	727
1	140	17	800
2	160	18	889
3	176	19	1000

Table 7. INTERNAL BOOSTER FREQUENCIES
(continued)

4	200	20	1067
5	222	21	1143
6	250	22	1231
7	276	23	1333
8	302	24	1455
9	333	25	1600
10	381	26	1778
11	444	27	2000
12	500	28	2286
13	552	29	2667
14	593	30	3200
15	667	31	4000

Booster PWM External Generation

When BST_SRC = 2, the booster PWM external generation mode is selected and the frequency is taken directly from the BSTSYNC device pin. There is no actual limitation in the resolution, but the same as indicated at PWM Internal Generation chapter is valid also here, the maximum frequency per booster phase should be 2 MHz and this implies maximum allowed frequency on BSTSYNC pin 4 MHz. The gate PWM is synchronized with either the rising or falling edge of the external signal depending on the BST_SRCINV bit value. The default POR value is "0" and corresponds to synchronization to the rising flank. BST_SRCINV equals "1" selects falling edge synchronization. Thanks to the possibility to invert external clock in the chip by SPI, up to 4-phase systems with shifted clock are supported with only 1 external clock.
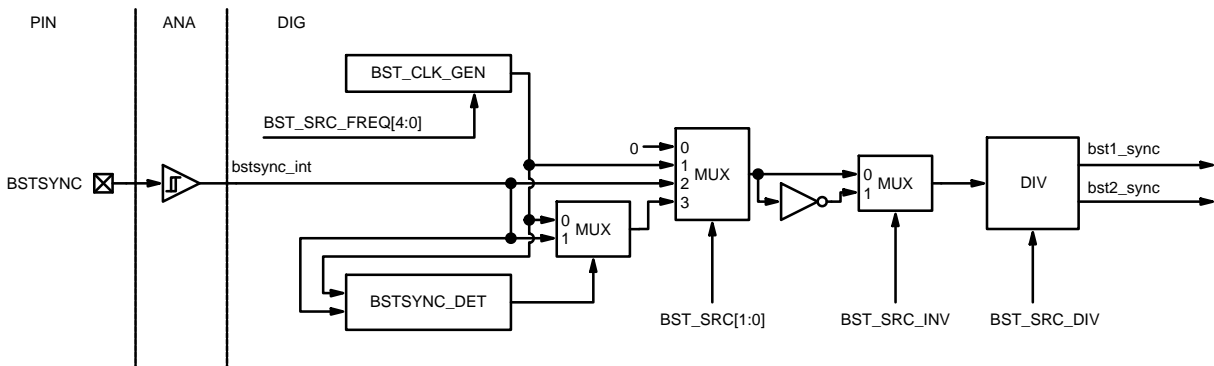

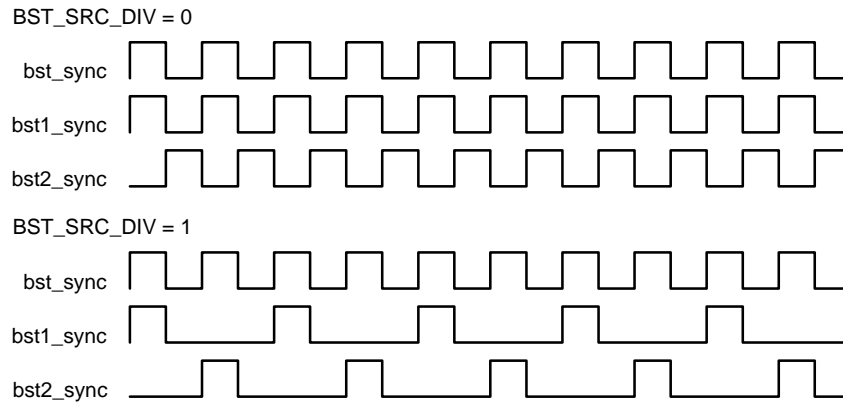**Figure 17. NCV78902 Booster Frequency Generation Block**

BST_SRC_DIV = 0

bst_sync

bst1_sync

bst2_sync

BST_SRC_DIV = 1

bst_sync

bst1_sync

bst2_sync

Figure 18. PWM Generator Clock Divider

Booster PWM Source Automatic Selection

When register BST_SRC = 3, the automatic booster PWM clock selection is activated. Switch sequence to internal clock is initialized when no rising edge on external source (bstsync_int on Figure 17) is detected within 3 consecutive rising edges of internal bst_sync clock. For this purpose, internal clock should be set to similar frequency as external source to ensure smooth transitions. Switch sequence to external clock is initialized when rising edge on external source (bstsync_int) is detected.

Table 8. BOOSTER PWM SOURCE SUMMARY

BST_SRC[1:0]	Booster Clock Source
0	Off
1	Internal
2	External
3	Auto External/Internal

Status bit BST_SYNCFAIL set to 1 indicates that there is an issue with booster external PWM clock. Bit is set when booster is supposed to run (at least one BSTx_EN control bit is set to 1), but PWM source is off (BST_SRC = 0) or external PWM source is selected (BST_SRC = 2 or 3) but no rising edge on BSTSYNC pin is detected within 3 consecutive rising edges of internal PWM clock set by BST_SRC_FREQ[4:0] register (even when not selected as primary PWM clock source, this internal clock is continuously running and checking synchronization of external PWM clock).

Booster PWM Min TOFF and Min TON Protection

As additional protection, the PWM duty cycle is constrained between a minimum and a maximum, defined per means of two parameters available in the device.

The PWM *minimum on-time* is programmable via BST_MIN_TON[1:0]: its purpose is to guarantee a minimum activation interval for the booster MOSFET gate, to insure full drive of the component and avoiding switching in the linear region. Please note that this does not imply that the PWM is always running even when not required by the

control loop, but means that whenever the MOSFET should be activated, then its on time would be at least the one specified. At the contrary when no duty cycle at all is required, then it will be zero.

The PWM *minimum off-time* is set via the parameter BST_MIN_TOFF[2:0]: this parameter is limiting the maximum duty cycle that can be used in the regulation loop for a defined period T_{PWM}:

$$Duty_{MAX} = \frac{\left(T_{PWM} - T_{OFFMIN}\right)}{T_{PWM}}$$

(eq. 3)

The main aim of a maximum duty cycle is preventing MOSFET shoot-through in cases the (transient) duty cycle would get too close to 100% of the MOSFET real switch-off characteristics. In addition, as a secondary effect, a limit on the duty cycle may also be exploited to minimize the inrush current when the load is activated. *Warning*: a wrong setting of the duty cycle constraints may result in unwanted system behavior. In particular, a too big BST_MIN_TOFF[2:0] may prevent the system to regulate the VBOOST with low battery voltages (VBAT). This can be explained by the simplified formula for booster steady state continuous mode:

$$V_{BOOST} \cong \frac{V_{BAT}}{(1 - Duty)} \Leftrightarrow Duty \cong 1 - \frac{V_{BAT}}{V_{BOOST}}$$

(eq. 4)

So in order to reach a desired VBOOST for a defined supply voltage, a certain duty cycle must be guaranteed.

Table 9. BOOSTER MINIMUM OFF TIME

BST_MIN_TOFF[2:0]	Min OFF Time (ns)
0	50
1	100
2	150
3	200
4	300
5	400
6	600
7	800

Table 10. BOOSTER MINIMUM ON TIME

BST_MIN_TON[1:0]	Min ON Time (ns)
0	100
1	150
2	200
3	300

Booster Compensator Model

A linear model of the booster controller compensator (block "A" Figure 13) is provided in this section. The protection mechanisms around are not taken into account. A type "2" network is taken into account at the VCOMP pin. The equivalent circuit is shown below:
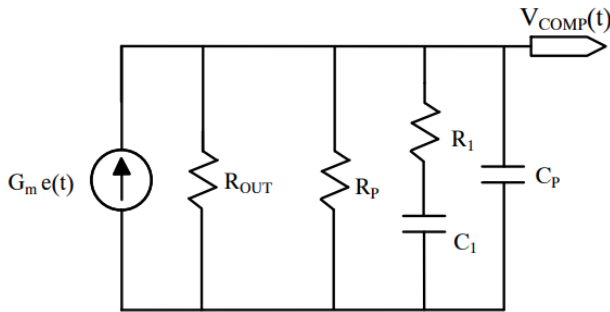

Figure 19. Booster Compensator Circuit with Type "2"

In the Figure, e(t) represents the control error, equals to the difference $V_{BST\_VSETPOINT}(t) - V_{BST}(t)$. "" is the trans-conductance error amplifier gain (see Table 6 – BOOST CONTROLLER – VOLTAGE REGULATION PARAMETERS section), while "R_{OUT}" is the amplifier internal output resistance (parameter EA_BLR in Table 6 – BOOST CONTROLLER – VOLTAGE REGULATION PARAMETERS section). By solving the circuit in Laplace domain the following error to V_{COMP} transfer function is obtained:

$$H_{COMP} = \frac{V_{COMP}(s)}{e(s)} = G_m R_{OUT} \frac{\tau_1 s + 1}{\tau_1 \tau_p s^2 + (\tau_p + \tau_{1p})s + 1}$$

(eq. 5)

The explanation of the parameters stated in the equation above follows:

$\tau_1 = R_1 C_1$
$\tau_p = R_1 C_p$
$\tau_{1p} = (R_1 + R_{OUT}) C_1$

This transfer function model can be used for closed loop stability calculations.

Booster PWM Skip Cycles

In case of light booster load, it is useful to reduce the number of effective PWM cycles in order to get a decrease of the input current inrush bursts and a less oscillating boost voltage. This can be obtained by using the "skip cycles" feature, programmable by SPI via BST_SKCL_THR[1:0] (see Table 6 – BOOST CONTROLLER – VOLTAGE REGULATION PARAMETERS section).

The selection defines the VCOMP voltage threshold below which the PWM is stopped, thus avoiding VBOOST oscillations in a larger voltage window.

Booster Multiphase Mode Principles

The NCV78902 device supports two booster phases, which are connected together to the same VBST node, sharing the boost capacitor block. Multiphase mode shows to be a cost effective solution in case of mid to high power systems, where bigger external BOM components would be required to bear the total power in one phase only with the same performances and total board size. In particular, the boost inductor could become a critical item for very high power levels, to guarantee the required minimum saturation current and RMS heating current.

Another advantage is the benefit from EMC point of view, due to the reduction in ripple current per phase and ripple voltage on the module input capacitor and boost capacitor. The picture below shows the (very) ideal case of 50% duty cycle, the ripple of the total module current ($I_{Lmp\_sum} = I_{L1mp} + I_{L2mp}$) is reduced to zero. The equivalent single phase current (I_{Lsp}) is provided as a graphical comparison.
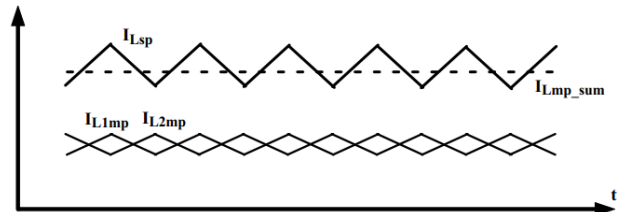

Figure 20. Booster Single Phase vs. Multiphase Example

Booster Multichip Connection Diagram and Programming

For high-power systems more NCV78902 devices can be combined to gain even more synchronized booster phases.

This section describes the steps both from hardware and SPI programming point of view to operate in multichip mode. Example of physical connection of two devices is provided in this section. From a hardware point of view, it is assumed that in multiphase mode (N boosters), each stage has the same external components. The following features have to be considered as well:

1. The compensation network is split between the two boosters' COMP pins according to Figure 21, to equalize the power distribution of each booster. For the best noise rejection, the compensation network area has to be surrounded by the GND plane. Please refer to the PCB Layout recommendations section for more general advices.
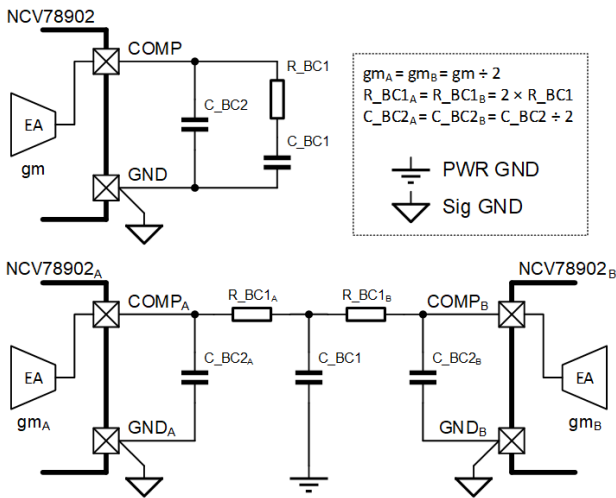
Figure 21. Compensation Network Connection for Single (Top) and Dual (Bottom) Device Operation

2. To synchronize the MOSFET gate PWM clock and needed phase shifts, the boosters must use the external clock generation (BSTSYNC), generated by the board MCU or external logic, according to the user-defined control strategy. The generic number of lines needed is equivalent to the number of devices. When two chips are combined, the slave device shall have BST_SRC_INV bit at '1' (clock polarity internal inversion active), whereas the master device will keep the BST_SRC_INV bit at '0' (= no inversion, default). On top of that, to get four phases with phase shift, the BST_SRC_DIV bit has to be at '1', meaning that gate clock is divided by two (please see Figure 17 and Figure 18 for more details).

3. Both devices should have error amplifier OTA set to the same gain value by means of register BST_OTA_GAIN[1:0]. Please note, that gain of both error amplifiers sums up.

4. Overvoltage settings of both devices should be set to the same level. Each device senses boost voltage via its VBST pin and reacts to the overvoltage situation independently. See also "Booster overvoltage shutdown protection" for more details on the protection mechanism and threshold.

<u>Booster Enable and Disable Control</u>

Each of the NCV78902 booster phases can be enabled/disabled directly by SPI via the corresponding BST1_EN or BST2_EN bit. The enable signal is the transition from "0" to "1"; the disable function is vice-versa. The status of the physical activation is contained in the flag BSTx_RUNNING: whenever the booster is running, the value of the flag is one, otherwise zero. It might in fact happen that despite the user *wanted* activation, the booster is stopped by the device in few cases:

1. Whenever the Thermal Shutdown TSD was triggers. Booster is re-enabled automatically when temperature falls below programmed thermal warning TW level. For more details see dedicated Diagnostic description chapter.

2. VDRV Undervoltage VDRV_UV was detected. After this error, the booster operation can be automatically resumed when automatic recovery is enabled by VDRV_UV_RCVR bit. For more details see dedicated Diagnostic description chapter.

3. Booster feedback failure was detected. This situation is indicated by BST_FBFAIL failure flag.

4. Booster internal hardware error was detected. This situation is indicated by BST_OSCFAIL failure flag.

<u>Booster Soft-start</u>

In order to limit inrush current during booster start up, the soft−start feature is available. Soft-start function ramps up booster voltage setpoint with defined step duration. Booster soft-start is controlled by the BST_SOFTSTART[2:0] register.

Table 11. BOOSTER SOFT−START

BST_SOFTSTART[2:0]	Step Duration (µs)
0	Soft-start disabled
1	12
2	20
3	28
4	36
5	44
6	52
7	60

Booster Diagnostic Description

- *Booster skip cycle:* indicates that skip cycle mode has been present in the regulation. BST_SKCL flag (latched) is contained in status register 0x36.

- *Booster overvoltage:* an overvoltage is detected by the booster control circuitry. BST_OV flag (lachted) is contained in status register 0x36.

- *Booster feedback failure:* when voltage at booster voltage feedback pin VBST is lost (detected by VBST voltage drop below BST_FBFAIL threshold, see Table 6 – BOOST CONTROLLER – VOLTAGE REGULATION PARAMETERS section), the booster is switched off. The failure is indicated by BST_FBFAIL status flag (reg. 0x36). To allow to use SEPIC topology, this protection can be switched off by register BST_FBFAIL_MASK[2:0] for defined number of periods after start according to the following table:

Table 12. BOOSTER FEEDBACK FAILURE MASKING

BST_FBFAIL_MASK[2:0]	Mask Time – Periods [–]
0	Never
1	4
2	16
3	64
4	256
5	1024
6	4096
7	Always

- *Booster oscillator failure:* BST_OSCFAIL fail flag is contained in status register 0x36 and indicates Booster internal hardware error. After detection of this error the Booster is switched off.
- *Booster VDRV undervoltage:* VDRV Undervoltage Lockout safety mechanism monitors sufficient voltage for booster MOSFETs and protects them by switching off the booster when VDRV voltage is too low. Detection level is set by VDRV_UV_THR[2:0] register (see Table 6 – VDRIVE: SUPPLY FOR BOOSTER MOSFET GATE DRIVE CIRCUIT AND BUCK LOW SIDE SWITCHES section for more details). When VDRV_UV_THR[2:0] = 0, the function is disabled. VDRV_UV (latched, reg. 0x36) flag indicates that protection has acted. Automatic reactivation of the booster after VDRV undervoltage can be enabled by VDRV_UV_RCVR bit.
- *Booster regulation status:* indicates for each booster phase individually that it runs in limitation mode. BSTx_REGSTATUS[1:0] registers are contained in status register 0x36. Coding of the register is the following:

Table 13. BOOSTER REGULATION STATUS

Booster Limitation Mode	BSTx_REGSTATUS[1:0]
Normal (Ireg comparator)	00
Limitation by current limit (Ilim comparator)	01
Limitation by minimum toff time (BST_MIN_TOFF)	10

- *Booster running:* the physical activation of the booster is displayed by the BSTx_RUNNING flag (non-latched, reg. 0x36). Please note this is different from the BSTx_EN control bits, which reports instead the *willing* to activate the booster. See also section "Booster Enable and Disable Control"/

General Diagnostic Description
- *Thermal Warning:* this mechanism detects a user-programmable junction temperature which is in principle close, but lower, to the chip maximum allowed, thus providing the information that some action (power de−rating) is required to prevent overheating that would cause Thermal Shutdown. The thermal warning flag (TW) is given in status register 0x20 and is latched. When VTEMP[8:0] raises to or above THERMAL_WARNING_THR[8:0] threshold, the TW flag is set. At power up the default thermal warning threshold is typically 150 °C (20 codes below TSD level).
- *Thermal Shutdown:* this safety mechanism intends to protect the device from damage caused by overheating, by disabling the booster. The diagnostic is displayed per means of the TSD bit in status register 0x20 (latched). Once occurred, the thermal shutdown condition is exited when the temperature drops below the thermal warning level, thus providing hysteresis for thermal shutdown recovery process. Booster is re-enabled automatically once thermal shutdown condition is exited. The application thermal design should be made as such to avoid the thermal shutdown in the worst case conditions. The thermal shutdown level is not user programmable and is factory trimmed (see ADC_TSD in Table 6 – ADC FOR MEASURING VBST, VCC, VDRV, VINT, TEMP section).
- *SPI Error:* in case of SPI communication errors the SPIERR bit in status register 0x20 is set. The bit is latched. For more details, please refer to section "SPI framing error".
- *EEPROM Error:* in case of read or write error during manipulation with EEPROM memory, the EEPROMERR bit in status register 0x20 is set. EEPROMERR is logical OR of EEPROM_WRITEFAIL and EEPROM_READFAIL errors.
- *Trimming Error:* TRIMERR bit in status register 0x20 is set when CRC_EEPROM_TRIM or CRC_EEPROM_CAL error is detected.
- *Command Reject:* CMD_REJECT bit in status register 0x20 is set when any EEPROM operation or write into EEPROM_DATA_WRITE[19:0] register is not accepted or when trial to write into SPI registers (except SWRESET, FSO_ENTER, FSO_EXIT, FSO_WDG_ENA[1:0] and FSO_WDG_CFG[1:0]) in FSO mode is made and rejected.
- *HW Reset:* the out of reset condition is reported through the HWR bit (latched, status register 0x20). This bit is set after each Power On Reset (POR) or SW reset (by SWRESET bit) and indicates the device is ready to operate.
- *FSO Mode:* presence in FSO mode is reported through the FSO bit in status register 0x20.
- *Frame Counter:* when valid SPI frame is received by the device, the register FRAME_CNT[3:0] (status register 0x20) is incremented. When actual value of the counter is 15, it will overflow to 0 after next valid SPI frame is received.
- *CSB Duration:* register CSB_DUR[19:0] (status registers 0x3D) reflects the last measured duration of CSB low pulse. CSB low pulse will be measured even in case of

invalid SPI frame. Resolution of the register is 1LSB = 62.5 ns. If CSB low pulse is longer than maximum what can be held by CSB_DUR[19:0] register (~65.5 ms), the register will keep maximum value.

Functional Mode Description

Overview of all functional modes is in accordance to the state diagram on Figure 22. Individual states are described below.
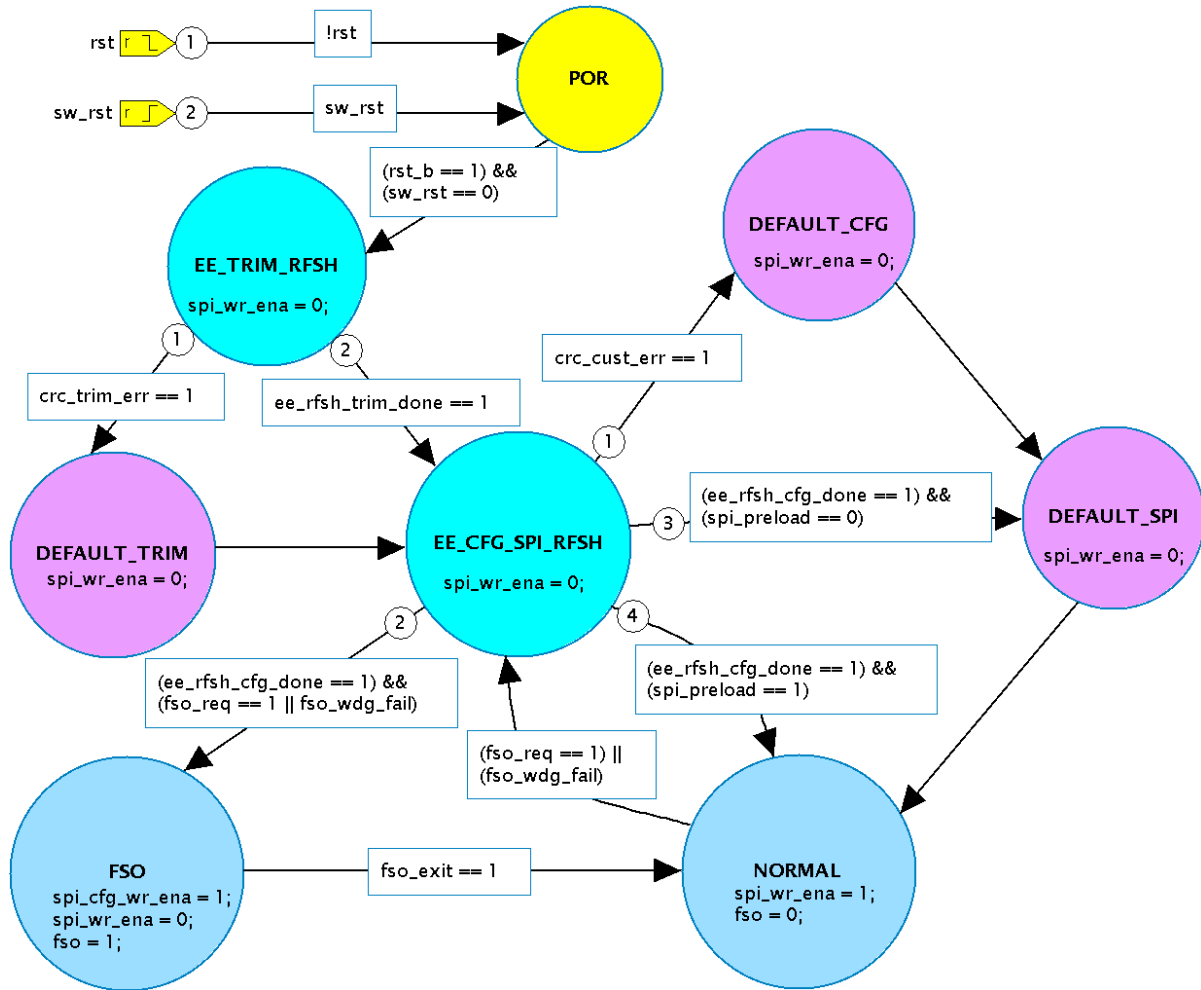

Figure 22. Functional Modes State Diagram

Reset

Asynchronous reset is caused either by POR (POR always causes asynchronous reset – transition to reset state) or by SWRESET SPI bit being written to 1.

Init and Normal Mode/FSO Mode

After the Reset, Trimming and Calibration constants are loaded from EEPROM into shadow registers and CRC check is performed. CRC check of trimming and calibration constants in shadow registers is performed also after each VTEMP measurement.

When EEPROM preload and CRC check of trimming constants in shadow registers fails also after the second trial, the CRC_EEPROM_TRIM (trimming data CRC check) error is raised and default trimming values are loaded into trimming shadow registers.

When CRC_EEPROM_TRIM (trimming data CRC check) or CRC_EEPROM_CAL (calibration data CRC

check) error is detected, SPI flag TRIMERR at address 0x20 is set to 1.

Configuration registers FSO_ENTER, FSO_WDG_ENA[1:0] and FSO_WDG_CFG[1:0] are loaded from EEPROM into SPI registers after the reset before entrance into FSO or Normal mode.

SPI bit FSO_ENTER controls entrance into FSO mode; if register value is 1, FSO mode will be entered, otherwise Normal mode will be entered.

Configuration register SPI_PRELOAD (EEPROM address 0x04), which is loaded from EEPROM after the reset, controls whether in Normal mode SPI registers will be loaded with values from EEPROM or with default SPI values. When SPI_PRELOAD is 1, SPI registers will be preloaded from EEPROM and this mode can be referred as Stand-Alone mode.

Customer EEPROM data are protected by CRC_EEPROM_CUST CRC check. When CRC_EEPROM_CUST (customer data CRC check) error is detected, SPI register EEPROM_READFAIL is set to 1 and default values will be loaded into SPI control registers.

Fail-Safe Operation Mode

FSO (Fail-Safe Operation) mode can be used for the purpose of **Fail-Safe** functionality (chip functionality definition in fail-safe mode when the external microcontroller functionality is not guaranteed).

FSO mode is entered in the following situations:
- After POR when control registers are preloaded and FSO_ENTER contains 1,
- From Normal mode when rising edge on FSO_ENTER SPI bit is detected and at the same moment SPI bit FSO_EXIT is 0,
- From Normal mode when Watchdog time-out elapses (indicated by FSO_WDG_FAIL).

When transitioning into FSO mode, the EEPROM refresh is performed. Please note, that when CRC error has been detected, SPI register EEPROM_READFAIL is set to 1, FSO mode is not entered and default values are loaded into SPI registers.

FSO mode can be exited when rising edge on FSO_EXIT SPI bit is detected and at the same moment SPI bit FSO_ENTER is 0.

FSO bit in status register 0x20 (and its mirror in SPI frame) is set to 1 when device is inside the FSO mode. FSO status bit is 0 outside the FSO mode.

In FSO mode write operations are allowed to SWRESET, FSO_ENTER, FSO_EXIT, FSO_WDG_ENA[1:0] and FSO_WDG_CFG[1:0] control registers at address 0x1D.

Stand-Alone Mode

Stand-Alone modes can be used for the purpose of default power-up operation of the chip (**Stand-Alone** functionality without external microcontroller or preloading of the registers with default content for default operation before microcontroller starts sending SPI commands for chip settings).

Stand-Alone mode is in fact Normal mode where SPI registers were preloaded from EEPROM after the reset and is entered in the following situation:
- After POR when configuration register SPI_PRELOAD, which is loaded from EEPROM, contains 1.

During SPI preload, the EEPROM refresh is performed. Please note, that when CRC error has been detected, SPI register EEPROM_READFAIL is set to 1 and default values are loaded into SPI registers.

In Stand-Alone mode, when SPI bus is not used, the SDO pin can be configured as failure indicator. See the following chapter for more details. Other unused SPI pins should be tied to GND.

Failure Output

SDO pin can be used as failure indicator (active low) when bit BST_FAIL_OUT at address 0x1D is set to 1.

SDO output will be asserted low when the following condition persists for more than 49 ms:

not SDO = (CSB pin = 1) and (*BSTERR* and BST_FAIL_OUT)

Please note that *BSTERR* is used also in SPI read frame in FAILURE_FLAGS[5:0] section, please see SPI Read Frame description for more details.

Meaning of the *BSTERR* is the following:

BSTERR = (not BST1_RUNNING and BST1_EN) or (not BST2_RUNNING and BST2_EN) or TSD or ((BSTx_REGSTATUS = 1 or BSTx_REGSTATUS = 2) and BST_ILIM_FMASK)

FSO Watchdog

Watchdog is restarted each time the valid SPI frame is received. When Watchdog is not properly restarted and time–out elapses, transition into FSO mode is started.

The watchdog can be configured and activated according to Table 14:

Table 14. WATCHDOG MODES

FSO_WDG_ENA[1:0]	Description
0	Watchdog disabled
1	Watchdog enabled after the first valid SPI frame
2	Watchdog enabled after NORMAL mode entrance
3	Watchdog enabled after NORMAL mode entrance with timeout 258.048 ±4.096 ms until the first valid SPI frame

FSO_WDG_CFG[1:0] control register defines the watchdog time-out:

Table 15. WATCHDOG TIME-OUT

FSO_WDG_CFG[1:0]	Min Timeout (ms)	Max Timeout (ms)
0	24.576	32.768
1	57.344	65.536
2	122.880	131.072
3	253.952	262.144

SPI INTERFACE

General

The serial peripheral interface (SPI) is used to allow an external microcontroller (MCU) to communicate with the device. NCV78902 acts always as a slave and it cannot initiate any transmission. The operation of the device is configured and controlled by means of SPI registers, which are observable for read and/or write from the master.

The NCV78902 SPI transfer size is 32 bits. Maximum communication SPI speed supported by NCV78902 is 4 MHz.

During an SPI transfer, the data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line (CLK) synchronizes shifting and sampling of the information on the two serial data lines: DO and DI. The DO signal is the output from the Slave (NCV78902), and the DI signal is the output from the Master.

A slave or chip select line (CSB) allows individual selection of a slave SPI device in a time multiplexed multiple-slave system.

The CSB line is active low. If an NCV78902 is not selected, DO is in high impedance state and it does not interfere with SPI bus activities. When the CSB line is low, the DO output is configured as push-pull to support higher communication speeds.

Since the NCV78902 always clocks data out on the falling edge and samples data in on rising edge of clock, the MCU SPI port must be configured to match this operation.

The implemented SPI allows connection to multiple slaves by means of star connection (CSB per slave.

An SPI star connection requires a bus = (3 + N) total lines, where N is the number of Slaves used, the SPI frame length is 32 bits per communication.
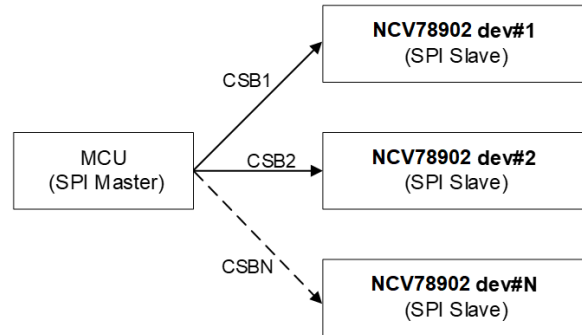

Figure 23. SPI Star Connection

SPI Transfer Format

Two types of SPI commands (to SDI pin of NCV78902) from the micro controller can be distinguished: "Write to a control register" and "Read from register (control or status)".

The frame protocol for the *write operation*:

Bits	[31]	[30:25]	[24:4]	[3:0]
SDI data	CMD	WRITE_ADDR[5:0]	WRITE_DATA[20:0]	CRC[3:0]
SDO data	SPIERR	LAST_ADDR[5:0]	LAST_DATA[20:0]	ECRC[3:0]

Figure 24. SPI Write Frame

Referring to the previous picture, the write frame coming from the master (into the SDI) is composed from the following fields:
- Bit[31] (MSB): CMD bit = 1 for write operation,
- Bits[30:25]: 6 bits WRITE ADDRESS field,
- Bits[24:4]: 21 bit DATA to write,
- Bits[3:0]: CRC field computed over CMD, WRITE_ADDR and WRITE_DATA in shown order from MSB to LSB.

Device in the same time replies to the master (on the DO):
- Bit[31] (MSB): SPI ERROR bit set in case last received SPI frame was invalid,
- Bits[30:25]: 6 bit ADDRESS (WRITE_ADDR or READ_ADDR) transmitted in previous valid SPI frame,

- Bits[24:4]: 21 bit actual DATA stored on address LAST_ADDR,
- Bits[3:0]: ECRC (extended CRC) computed over SPIERR, LAST_DATA, LAST_ADDR, CMD (which has to be extended to 2 bits by one zero from left) and WRITE_ADDR in shown order from MSB to LSB.

In case the write operation is the first frame after power-on-reset, address of NOP register is used as LAST_ADDR.

If CRC in the frame is wrong, device will not perform command and <SPIERR> flag will be set.

The frame protocol for the *read operation*:

Bits	[31]	[30:25]						[24:4]	[3:0]
SDI data	CMD	READ_ADDR[5:0]						IGNORED[20:0]	CRC[3:0]
SDO data	SPIERR	FAILURE_FLAGS[5:0]						READ_DATA[20:0]	ECRC[3:0]
		HWR	TW	FSO	0	0	BSTERR		

Figure 25. SPI Read Frame

Referring to the previous picture, the read frame coming from the master (into the SDI) is composed from the following fields:

- Bit[31] (MSB): CMD bit = 0 for read operation,
- Bits[30:25]: 6 bits READ ADDRESS field,
- Bits[24:4]: 21 bits zeroes field,
- Bits[3:0]: 4 bits CRC field computed over CMD, READ_ADDR and IGNORED in shown order from MSB to LSB.

Device in the same frame provides to the master (on the DO):

- Bit[31] (MSB): SPI ERROR bit set in case last received SPI frame was invalid,
- Bits[30:25]: FAILURE_FLAGS[5:0] field composed from:
    - HWR flag (mirror of HWR SPI flag),
    - TW flag (mirror of TW SPI flag),
    - FSO flag (mirror of FSO SPI flag),
    - BSTERR fail status; please see Failure Output chapter to see details from which bits these fail status indicators are composed,
- Bits[24:4]: actual data from address READ_ADDR,
- Bits[3:0]: ECRC (extended CRC) computed over SPIERR, FAILURE_FLAGS, READ_DATA, CMD (which has to be extended to 2 bits by one zero from left) and READ_ADDR in shown order from MSB to LSB.

Read frame provides data from the required address to the output within the same frame (in frame response), thus achieving the lowest communication latency.

CRC Calculation

Received and transmitted frames are protected by CRC with following parameters:

- CRC length is 4 bits,
- CRC polynomial 0x9 (Koopman's notation; x4+x+1),
- CRC initialization value 0xF.

SPI Framing Error

SPI communication framing error is detected by the NCV78902 in the following situations:

- Not zero or 32 CLK pulses are received during the active-low CSB signal;
- CRC calculated from all received bits is not equal to zero;
- Write operation to read only register was performed.

Once an SPI error occurs, the <SPIERR> flag can be reset only by reading the status register in which it is contained by valid SPI frame.

Incoming SPI messages from NCV78902 to MCU shall be validated by ECRC (extended CRC) to guarantee correct transmission and data representation.

CRC Code Example

```c
#include <stdint.h>

// Calculates 4 bit CRC from given data array "data" and data byte count "length". Returns 4 bit CRC value
uint8_t CalcCRCfromByteArray(uint8_t* data, uint8_t length) {
    static const uint8_t CRC_POLY = 0x03;    // Polynomial x^4 + x + 1 (0x03 Normal representation, 0x09 Koopman)
    static const uint8_t CRC_INIT = 0x0F;    // Initialization value

    uint8_t crc = 0;                         // CRC register
    uint8_t bit = 0;                         // Bit to be shifted into CRC register

    // Begin CRC calculation byte by byte
    for(uint8_t byteIdx = 0; byteIdx < length; byteIdx++) {
        if(byteIdx == 0) {
            // Initialize CRC register - Shift in the first 4 highest bits (starting from CMD),
            for(int8_t bitIdx = 7; bitIdx >= 4; bitIdx--) {
                bit = (data[byteIdx] >> bitIdx) & 0x01;
                crc = (crc << 1) | bit;
            }
            crc ^= CRC_INIT;                 // XOR with CRC initial value
        }

        // Continue from bit 3...0 after Init in case of First byte is processed
        // Else process all 8 bits (7...0) of given byte
        for (int8_t bitIdx = (byteIdx == 0 ? 3 : 7); bitIdx >= 0; bitIdx--) {
            bit = (data[byteIdx] >> bitIdx) & 0x01;
            crc = (crc << 1) | bit;
            if (crc & 0x10) {                // Check CRC register popout bit
                crc ^= CRC_POLY;
            }
        }
    }

    return (crc & 0x0F);                     // Return CRC - only the lower 4 bits
}

// CRC Calculation from masterOUT message
uint8_t CalcCRC(uint32_t masterOUT) {
    // Create data byte array with expected structure for CRC calculation
    uint8_t data[4] = {0};                   // 4 data bytes
    data[0] = (masterOUT >> 24) & 0xFF;      // Bits 31...24 (31 = CMD)
    data[1] = (masterOUT >> 16) & 0xFF;      // Bits 23...16 (23 = write_data/ignored[19])
    data[2] = (masterOUT >> 8) & 0xFF;       // Bits 15...8  (15 = write_data/ignored[11])
    data[3] = masterOUT & 0xF0;              // Bits 7...4   (7 = write_data/ignored[3])
                                             // Bits 3...0   (CRC padding = 0)
    return CalcCRCfromByteArray(data, 4);
}

// ECRC Calculation from device response (masterIN) and part of masterOUT message
uint8_t CalcECRC(uint32_t masterOUT, uint32_t masterIN) {
    // Create data byte array with expected structure for CRC calculation
    uint8_t data[5] = {0};                   // 5 data bytes
    data[0] = (masterIN >> 24) & 0xFF;       // Bits 39...32 (39 = SPIERR)
    data[1] = (masterIN >> 16) & 0xFF;       // Bits 31...24 (31 = last_/read_data[19])
    data[2] = (masterIN >> 8) & 0xFF;        // Bits 23...16 (23 = last_/read_data[11])
    data[3] = (masterIN & 0xF0) |            // Bits 15...12 (last_/read_data[3]...last_/read_data[0])
              (masterOUT >> 29) & 0x07;      // Bits 11...8  (11 = 0 (extended CMD), 10 = CMD)
    data[4] = ((masterOUT >> 25) & 0x0F) << 4;  // Bits 7...4   (write_/read_addr[3]...[0])
                                             // Bits 3...0   (ECRC calculation padding = 0)
    return CalcCRCfromByteArray(data, 5);
}

//******************************************************************************//
// Example CRC/ECRC calculation - Read Register 0x3F (REVID) after device power up
// ...
uint32_t masterOUT = 0x7e000000;  // Master out message (CMD = 0; read_addr = 0x3F, CRC = 0 [placeholder])
uint8_t crc = CalcCRC(masterOUT); // Expected CRC result = 0x4
masterOUT |= (crc & 0x0F);        // Set lowest 4 bits to calculated CRC value (masterOUT = 0x7e000004)

// Write data to SPI while reading device in frame response (into masterIN variable)
uint32_t masterIN = spiTransfer(masterOUT);

// Expected  response of NCV78902 (0x4000208d) - HWR set; REVID = 0x208; ECRC = 0xD

uint8_t ecrc_response = (masterIN & 0x0F);        // Read lowest 4 bits of response - ECRC
uint8_t ecrc_calc = CalcECRC(masterOUT, masterIN); // Check ECRC validity (should match response ECRC)

if(ecrc_calc != ecrc_response) {
        // ...Handle ECRC error
}
// ...Process Device Response
// ...
```

SPI Address Map

	ADDR	bit20	bit19	bit18	bit17	bit16	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0x00									NOP[20:0]												
1	0x02																					
2	0x02																					
3	0x03																					
4	0x04																					
5	0x05																					
6	0x06																					
7	0x07																					
8	0x08																					
9	0x09																					
10	0x0A																					
11	0x0B																					
12	0x0C																					
13	0x0D																					
14	0x0E									BST1_SLP_CTRL[2:0]			BST1_COMP_DIV[2:0]			BST1_VLIM_THR[7:0]						
15	0x0F									BST2_SLP_CTRL[2:0]			BST2_COMP_DIV[2:0]			BST2_VLIM_THR[7:0]						
16	0x10																					
17	0x11	BST_ILIM_FMASK	VDRV_UV_RCVR		VDRV_UV_THR[2:0]			BST_OTA_GAIN[1:0]		BST_MIN_TON[1:0]		BST_MIN_TOFF[2:0]				BST_SRC_FREQ[4:0]			BST_SRC_DIV	BST_SRC_INV	BST_SRC[1:0]	
18	0x12	BST_SKCL_THR[1:0]		BST_SOFTSTART_UV		BST_SOFTSTART[2:0]		BST_OV_REACT[1:0]		BST_OV_SD[2:0]				BST_VSETPOINT[6:0]						BST2_EN	BST1_EN	
19	0x13																		BST_FBFAIL_MASK[2:0]			
20	0x14																					
21	0x15																					
22	0x16																					
23	0x17																					
24	0x18																					
25	0x19																					
26	0x1A									OSC_CAL[4:0]					THERMAL_WARNING_THR[8:0]							
27	0x1B									EEPROM_DATA_WRITE[19:0]												
28	0x1C														EEPROM_ADDRESS[3:0]				EEPROM_CTRL[3:0]			
29	0x1D												BST_FAIL_OUT		FSO_WDG_CFG[1:0]		FSO_WDG_ENA[1:0]		FSO_EXIT	FSO_ENTER		SWRESET
30	0x1E																					
31	0x1F																					
32	0x20								TRIMERR	EEPROMERR		SPIERR	CMD_REJECT	FRAME_CNT[3:0]			TSD		TW	FSO	HWR	
33	0x21																					
34	0x22																					
35	0x23																					
36	0x24																					
37	0x25																					
38	0x26																					
39	0x27																					
40	0x28																					
41	0x29																					
42	0x2A																					
43	0x2B																					
44	0x2C																					
45	0x2E																					
46	0x2E																					
47	0x2F																					
48	0x30																					
49	0x31																					
50	0x32																					
51	0x33																					
52	0x34																					
53	0x35																					
54	0x36							BST_SKCL	BST_OV	BST_SYNCFAIL	BST_FBFAIL	BST_OSCFAIL	VDRV_UV				BST2_REGSTATUS[1:0]		BST2_RUNNING	BST1_REGSTATUS[1:0]		BST1_RUNNING	
55	0x37													VBST[8:0]								
56	0x38																					
57	0x39																					
58	0x3A																					
59	0x3B				VCC[8:0]										VINT[8:0]							
60	0x3C				VDRV[8:0]										VTEMP[8:0]							
61	0x3D									CSB_DUR[19:0]												
62	0x3E									EEPROM_DATA_READ[19:0]												
63	0x3F						EEPROM_LOCK_CUST	EEPROM_WRITEFAIL	EEPROM_READFAIL	EEPROM_BUSY			REVID[12:0]									

	Write
	Write FSO
	Read Only
	Read Only Clear by Read
	NOP

Figure 26. NCV78902 SPI Address Map

Default value of all SPI registers after POR is 0x00 if not specified explicitly.

SPI register SPI_REVID[12:0] is used to track the silicon version, following encoding mechanism is used:

- REVID[12:8]: Device ID for NCV78902 = 00010 [binary]

- REVID[7:6]: Option ID
- REVID[5:3]: Full Mask Version
- REVID[2:0]: Metal Tune

Table 16. SPI MAP BIT DEFINITION

Symbol	MAP Position	Description
REGISTER 0x00 (CR): NOP REGISTER		
NOP[20:0]	Bits [20:0] – ADDR_0x00	NOP Register (Read/Write Operation Ignored)
REGISTER 0x0E (BOOST1) or 0x0F (BOOST2) (CR): BOOSTx CONFIGURATION		
BST1_SLP_CTRL[2:0]	Bits [13:11] – ADDR_0x0E	Booster Phase Slope Control
BST1_COMP_DIV[2:0]	Bits [10:8] – ADDR_0x0E	Booster Phase Division factor from the COMP pin
BST1_VLIM_THR[7:0]	Bits [7:0] – ADDR_0x0E	Booster Phase Current limitation threshold
REGISTER 0x11 (CR): BOOST CONFIGURATION		
BST_ILIM_FMASK	Bit 20 – ADDR_0x11	Adding the ILIM (current limitation) status into BSTERR for Failure Output and for SPI read frame FAILURE_FLAGS[5:0] section
VDRV_UV_RCVR	Bit 19 – ADDR_0x11	Automatic Recovery after VDRIVE Undervoltage
VDRV_UV_THR[2:0]	Bits [18:16] – ADDR_0x11	VDRIVE Undervoltage threshold
BST_OTA_GAIN[1:0]	Bits [15:14] – ADDR_0x11	Booster Error Amplifier Gain
BST_MIN_TON[1:0]	Bits [13:12] – ADDR_0x11	Booster Minimal TON time
BST_MIN_TOFF[1:0]	Bits [11:9] – ADDR_0x11	Booster Minimal TOFF time
BST_SRC_FREQ[4:0]	Bits [8:4] – ADDR_0x11	Booster Internal clock frequency
BST_SRC_DIV	Bit 3 – ADDR_0x11	Booster clock frequency divided by 1 or 2
BST_SRC_INV	Bit 2 – ADDR_0x11	Booster clock inversion
BST_SRC[1:0]	Bits [1:0] – ADDR_0x11	Booster clock source
REGISTER 0x12 (CR): BOOST CONFIGURATION		
BST_SKCL_THR[1:0]	Bits [20:19] – ADDR_0x12	Booster Skip cycle
BST_SOFTSTART_UV	Bit 18 – ADDR_0x12	Activation of Soft–start after VDRIVE Undervoltage
BST_SOFTSTART[2:0]	Bits [17:15] – ADDR_0x12	Booster Soft–start
BST_OV_REACT[1:0]	Bits [14:13] – ADDR_0x12	Booster overvoltage reactivation level
BST_OV_SD[2:0]	Bits [12:10] – ADDR_0x12	Booster overvoltage level
BST_VSETPOINT[6:0]	Bits [9:3] – ADDR_0x12	Booster voltage setpoint
BST2_EN	Bit 1 – ADDR_0x12	Booster Phase 2 Enable
BST1_EN	Bit 0 – ADDR_0x12	Booster Phase 1 Enable
REGISTER 0x13 (CR): SETTINGS		
BST_FBFAIL_MASK[2:0]	Bits [2:0] – ADDR_0x13	Masking of feedback fail for SEPIC use
REGISTER 0x1A (CR): OSCILLATOR CALIBRATION & THERMAL WARNING SETTINGS		
OSC_CAL[4:0]	Bits [13:9] – ADDR_0x1A	Calibration of the internal Oscillator. Signed, coded as two's complement
THERMAL_WARNING_THR[8:0]	Bits [8:0] – ADDR_0x1A	Thermal Warning Threshold Settings
REGISTER 0x1B (CR): EEPROM OPERATION		
EEPROM_DATA_WRITE[19:0]	Bits [19:0] – ADDR_0x1B	EEPROM Data to be Written

Table 16. SPI MAP BIT DEFINITION (continued)

Symbol	MAP Position	Description
REGISTER 0x1C (CR): EEPROM OPERATION		
EEPROM ADDRESS[3:0]	Bits [7:4] – ADDR_0x1C	EEPROM Address
EEPROM_CTRL[3:0]	Bits [3:0] – ADDR_0x1C	EEPROM Command
REGISTER 0x1D (CR): FSO MODE CONFIGURATION		
BST_FAIL_OUT	Bit 9 – ADDR_0x1D	Providing the Booster failure BSTERR to Failure Output
FSO_WDG_CFG[1:0]	Bits [6:5] – ADDR_0x1D	Watchdog time–out configuration
FSO_WDG_ENA[1:0]	Bits [4:3] – ADDR_0x1D	Watchdog mode
FSO_EXIT	Bit 2 – ADDR_0x1D	FSO mode exit command
FSO_ENTER	Bit 1 – ADDR_0x1D	FSO mode enter command
SWRESET	Bit 0 – ADDR_0x1D	Software Reset
REGISTER 0x20 (SR): DIAGNOSTIC		
TRIMERR	Bit 11 – ADDR_0x20	Trimming or Calibration EEPROM data CRC check failed
EEPROMERR	Bit 10 – ADDR_0x20	Logical OR of EEPROM_WRITEFAIL and EEPROM_READFAIL errors
SPIERR	Bit 9 – ADDR_0x20	SPI Error Flag, Latched
CMD_REJECT	Bit 8 – ADDR_0x20	EEPROM operation or write into EEPROM_DATA_WRITE[19:0] register not accepted or trial to write not allowed SPI registers in FSO mode rejected, Latched
FRAME_CNT[3:0]	Bits [7:4] – ADDR_0x20	SPI Frame Counter
TSD	Bit 3 – ADDR_0x20	Thermal Shutdown Flag, Latched
TW	Bit 2 – ADDR_0x20	Thermal Warning Flag
FSO	Bit 1 – ADDR_0x20	FSO mode indicator
HWR	Bit 9 – ADDR_0x20	Hardware Reset Flag, Latched
REGISTER 0x36 (SR): BOOST DIAGNOSTIC		
BST_SKCL	Bit 14 – ADDR_0x36	Booster Skip Cycle mode indicator, Latched
BST_OV	Bit 13 – ADDR_0x36	Booster Overvoltage detected, Latched
BST_SYNCFAIL	Bit 12 – ADDR_0x36	Booster External PWM Clock Failure
BST_FBFAIL	Bit 11 – ADDR_0x36	Booster Feedback Failure
BST_OSCFAIL	Bit 10 – ADDR_0x36	Booster Hardware error
VDRV_UV	Bit 9 – ADDR_0x36	VDRV Undervoltage detected
BST2_REGSTATUS[1:0]	Bits [5:4] – ADDR_0x36	Booster Phase 2 Regulation status
BST2_RUNNING	Bit 3 – ADDR_0x36	Booster Phase 2 Running indicator
BST1_REGSTATUS[1:0]	Bits [2:1] – ADDR_0x36	Booster Phase 1 Regulation status
BST1_RUNNING	Bit 0 – ADDR_0x36	Booster Phase 1 Running indicator
REGISTER 0x37 (SR): BOOST DIAGNOSTIC		
VBST[8:0]	Bits [8:0] – ADDR_0x37	Output of VBST ADC measurement
REGISTER 0x3B (SR): ADC		
VCC[8:0]	Bits [18:10] – ADDR_0x3B	Output of VCC ADC measurement
VINT[8:0]	Bits [8:0] – ADDR_0x3B	Output of VINT ADC measurement
REGISTER 0x3C (SR): ADC		
VDRV[8:0]	Bits [18:10] – ADDR_0x3C	Output of VDRV ADC measurement
VTEMP[8:0]	Bits [8:0] – ADDR_0x3C	Output of VTEMP ADC measurement

Table 16. SPI MAP BIT DEFINITION (continued)

Symbol	MAP Position	Description
REGISTER 0x3D (SR): DIAGNOSTIC		
CSB_DUR[19:0]	Bits [19:0] – ADDR_0x3D	Measured Duration of CSB low pulse
REGISTER 0x3E (SR): EEPROM		
EEPROM_DATA_READ[19:0]	Bits [19:0] – ADDR_0x3E	EEPROM Read Data
REGISTER 0x3F (SR): EEPROM & REVID		
EEPROM_LOCK_CUST	Bit 16 – ADDR_0x3F	EEPROM Customer Data Locked
EEPROM_WRITEFAIL	Bit 15 – ADDR_0x3F	EEPROM Data Write Failure
EEPROM_READFAIL	Bit 14 – ADDR_0x3F	EEPROM Data CRC check Failure, Latched
EEPROM_BUSY	Bit 13 – ADDR_0x3F	EEPROM Busy
REVID[12:0]	Bits [12:0] – ADDR_0x3F	Revision ID of the Device

NCV78902

ADDR	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x04			BST_FAIL_OUT			FSO_WDG_CFG[1:0]		FSO_WDG_ENA[1:0]		FSO_ENTER	SPI_PRELOAD	THERMAL_WARNING_THR[8:0]								
0x05		BST_SOFTSTART_UV	BST_ILIM_FMASK	BST_OTA_GAIN[1:0]		BST_SOFTSTART[2:0]			BST_OV_REACT[1:0]		BST_OV_SD[2:0]			BST_VSETPOINT[6:0]						
0x06	VDRV_UV_RCVR	VDRV_UV_THR[2:0]			BST_SKCL_THR[1:0]		BST_MIN_TON[1:0]		BST_MIN_TOFF[2:0]			BST_SRC_FREQ[4:0]					BST_SRC_DIV	BST_SRC_INV	BST_SRC[1:0]	
0x07			BST_FBFAIL_MASK[2:0]			BST1_SLP_CTRL[2:0]			BST1_COMP_DIV[2:0]			BST1_VLIM_THR[7:0]								BST1_EN
0x08						BST2_SLP_CTRL[2:0]			BST2_COMP_DIV[2:0]			BST2_VLIM_THR[7:0]								BST2_EN
0x09	EEPROM_LOCK_CUST				CRC_EEPROM_CUST[15:0]															

	Customer
	unused

Figure 27. NCV78902 EEPROM Memory Map

EEPROM MEMORY

EEPROM memory serves as persistent storage for Customer configuration and for **onsemi** calibration, trimming and test data. EEPROM memory is organized as 51 words, each 20 bits wide. The access to the memory is word-based.

EEPROM Operations

The NCV78902 supports following operations with EEPROM memory:

- EEPROM_CTRL[3:0] = 0xxx [binary]: EEPROM in Power-down state (no operation)
- EEPROM_CTRL[3:0] = 1xxx [binary]: **Enable**
- EEPROM_CTRL[3:0] = 1001 [binary]: **Read** – data addressed by SPI register EEPROM_ADDRESS[3:0] become available in SPI register EEPROM_DATA_READ[19:0] after end of Read operation
- EEPROM_CTRL[3:0] = 1110 [binary]: **Unlock Write**
- EEPROM_CTRL[3:0] = 1010 [binary]: **Write** – data in EEPROM_DATA_WRITE[19:0] SPI register will be written into address EEPROM_ADDRESS[3:0]

EEPROM Read Operation

The correct sequence to Read data from EEPROM memory should be the following:

- Write **'Enable'** (0x8hex) into EEPROM_CTRL[3:0] SPI register to bring EEPROM memory into powered state
- Read EEPROM_CTRL[3:0] SPI register and check that it is **'Enable'** (0x8hex)
- Wait until EEPROM_BUSY is 0 (EEPROM power–up time is app. 30 μs)
- Write required address into EEPROM_ADDRESS[3:0] SPI register and write **'Read'** (0x9hex) into EEPROM_CTRL[3:0] SPI register to perform Read command
- Read EEPROM_CTRL[3:0] SPI register and check that it is **'Read'** (0x9hex) and read EEPROM_ADDRESS[3:0] SPI register and check that it is correct
- Read data at EEPROM_DATA_READ[19:0] SPI register
- Repeat reading from all required addresses
- Write 'Power down' (0x0hex) into EEPROM_CTRL[3:0] SPI register to put EEPROM memory into power-down mode
- To check that all content was written correctly,

EEPROM Write Operation

The correct sequence to Write data from EEPROM memory should be the following:

- Write **'Enable'** (0x8hex) into EEPROM_CTRL[3:0] SPI register to bring EEPROM memory into powered state
- Read EEPROM_CTRL[3:0] SPI register and check that it is **'Enable'** (0x8hex)
- Wait until EEPROM_BUSY is 0 (EEPROM power-up time is app. 30 μs)
- Write required data into EEPROM_DATA_WRITE[19:0] SPI register
- Read data at EEPROM_DATA_WRITE[19:0] SPI register and check if the content is correct
- Write **'Unlock Write'** (0xEhex) into EEPROM_CTRL[3:0] SPI register to enable write
- Read EEPROM_CTRL[3:0] SPI register and check that it is **'Unlock Write'** (0xEhex)
- Write required address into EEPROM_ADDRESS[3:0] SPI register and write **'Write'** (0xAhex) into EEPROM_CTRL[3:0] SPI register to perform Write command
- Read EEPROM_CTRL[3:0] SPI register and check that it is **'Write'** (0xAhex) and read EEPROM_ADDRESS[3:0] SPI register and check that it is correct
- Wait until EEPROM_BUSY is 0 (EEPROM word programming time is app. 9.2 ms)
- Check that EEPROM_WRITEFAIL is 0. Discard the device if EEPROM_WRITEFAIL is 1.
- Repeat writing into all required addresses
- Read and check EEPROM data from all written addresses
- Write 'Power down' (0x0hex) into EEPROM_CTRL[3:0] SPI register to put EEPROM memory into power-down mode

To provide extra safety, CRC protection is implemented to secure EEPROM memory content. The following CRC check is implemented:

CRC_EEPROM_CUST[15:0] (ADDR_0x9hex) is calculated over all EEPROM Customer data, starting from MSB bit on EEPROM address 4 and ending at bit 16 of EEPROM address 9.

CRC algorithm with following parameters is used:

- CRC length is 16 bits,
- CRC polynomial 0xBAAD (Koopman's notation; $x16+x14+x13+x12+x10+x8+x6+x4+x3+x+1$),
- CRC initialization value 0xFFFF.

External microcontroller should calculate its own CRC from the appropriate EEPROM data and verify that calculated CRC matches with CRC stored in EEPROM.

PCB LAYOUT RECOMMENDATIONS

This section contains instructions for the NCV78902 PCB layout application design. Although this guide does not claim to be exhaustive, these directions can help the developer to reduce application noise impact and insuring the best system operation. All important areas are highlighted on the following picture:
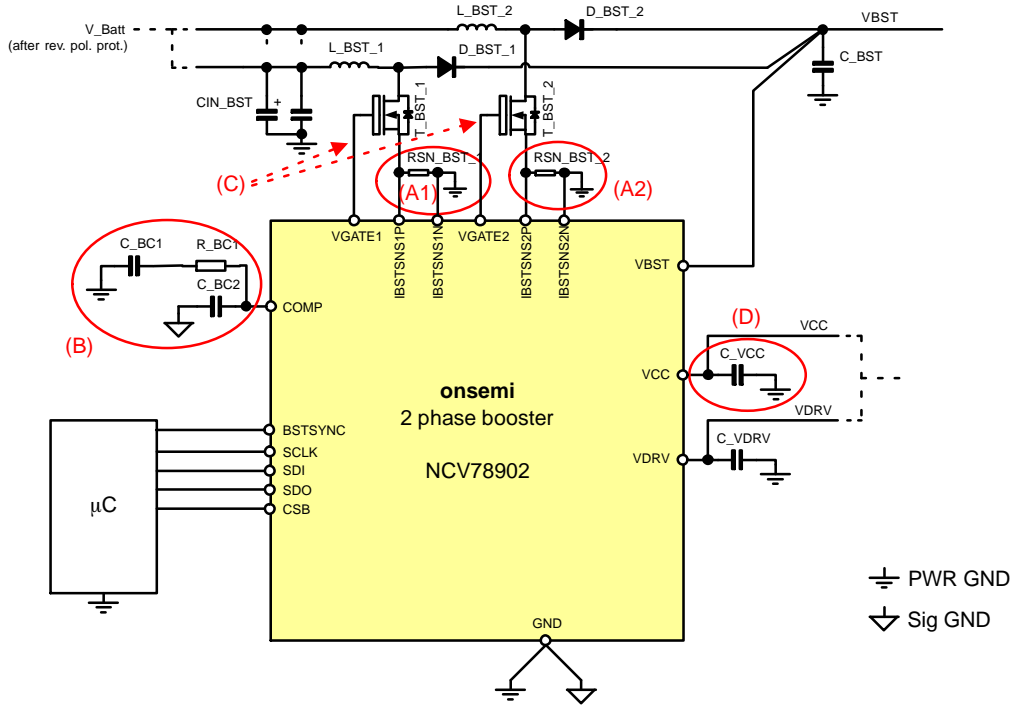

Figure 28. NCV78902 Application Critical PCB Areas

PCB Layout: Booster Current Sensing – Area (A1, A2)

The booster current sensing circuit is used both by the loop regulation and the current limitation mechanism. In case of current sensing over sensing resistor, it relies on a low voltage comparator, which triggers with respect to the sense voltage across the external resistors RSN_BST_1/2. In order to maximize power efficiency (= minimum losses on the sense resistor), the threshold voltage is rather low, with a maximum setting of 100 mV typical. This area may be affected by the MOSFET switching noise if no specific care is taken. The following recommendations are given:

1. Use a four terminals current sense method as depicted in the figure below. The measurement PCB tracks should run in parallel and as close as possible to each other, trying to have the same length. The number of vias along the measurement path should be minimized;
2. Place RSN_BST_1/2 sufficiently close to the MOSFET source terminal;
3. The MOSFET's dissipation area should be stretched in a direction away from the sense resistor to minimize resistivity changes due to heating;
4. If the current sense measurement tracks are interrupted by series resistors or jumpers (once as a maximum) their value should be matched and low ohmic (pair of 0 Ω to 47 Ω max) to avoid errors due

to the comparator input bias currents. However, in case of high application noise, a PCB re-layout without RC filters is always recommended.
5. Avoid using the board GND as one of the measurement terminals as this would also introduce errors.
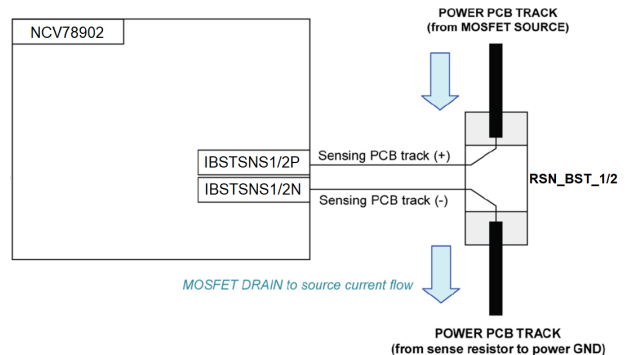
Figure 29. Four Wires Method for Booster Current Sensing Circuit

PCB Layout: Booster Compensation Network – Area (B)

The compensation network must be placed very close to the chip to avoid noise capturing. Its ground has to be

connected directly to the chip ground pin to avoid noise coming from other portions of the PCB ground. In addition a ground ring shall provide extra shielding ground around.

PCB Layout: VGATE Signals – Area (C)

It has to be ensured that VGATE signals do not interfere with other signals like COMP or input of the IMAX or IREG comparators.

PCB Layout: VDD Connections – Area (D)

The VDD decoupling capacitor has to be connected directly to the VDD and ground pins with separate PCB tracks to avoid coupling of the ground shift on the PCB into the chip.

PCB Layout: Additional EMC Recommendations on Loops

It is suggested in general to have a good metal connection to the ground and to keep it as continuous as possible, not interrupted by resistors or jumpers. In additions, PCB loops for power lines should be minimized. A simplified application schematic is shown in the next figure to better focus on the theoretical explanation. When a DC voltage is applied to the VBB, at the left side of the boost inductor L_BOOST, a DC voltage also appears on the right side of L_BUCK and on the C_BUCK. However,

due to the switching operation (boost and buck), the applied voltage generates AC currents flowing through the red area (1). These currents also create time variable voltages in the area marked in green (2). In order to minimize the radiation due to the AC currents in area 1, the tracks' length between L_BOOST and the pair L_BUCK plus C_BUCK must be kept low. At the contrary, if long tracks would be used, a bigger parasitic capacitance in area 2 would be created, thus increasing the coupled EMC noise level.
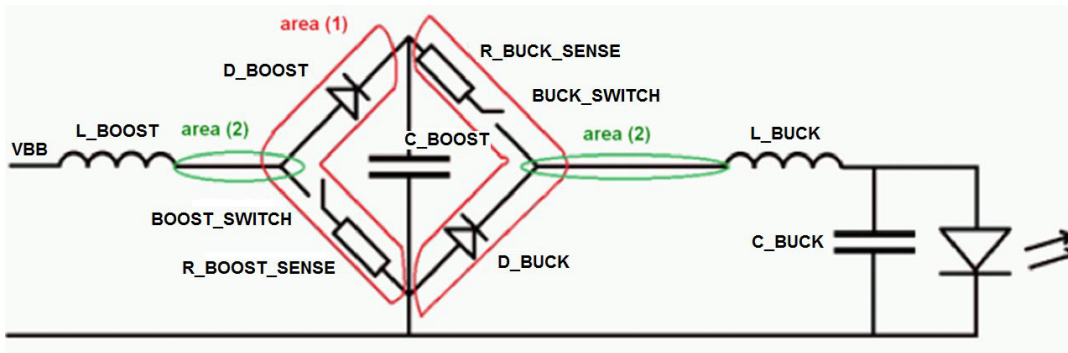
Figure 30. PCB AC Current Lines (1) and AC Voltage Nodes (2)

PCB Layout: Spacing between High and Low Voltage Pins

In case of typical application with current sensing over sensing resistor RSN_BST_1/2, high voltage pin VBST (pin 16) is located directly next to the pin with low voltage IBSTSNS1P (pin 15). In case of sensing over MOSFET RDSon, switching signal with levels between high booster voltage and GND will appear on pin IBSTSNS1P (pin 15) which is located between high voltage pin VBST (pin 16) and low voltage pin IBSTSNS1N (pin 14). In either case, if there is a need to improve spacing between high and low voltage pins due to requirements of IPC2221 or similar standard, it can be considered to design soldering footprint with narrower pads than recommended in Soldering footprint.

ORDERING INFORMATION

Device	Marking	Package*	Shipping†
NCV78902DE0R2G	N78902-1	TSSOP–16 WB (Pb-Free)	4000 / Tape & Reel

*For additional information on our Pb–Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
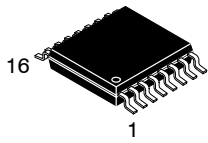
TSSOP−16 WB
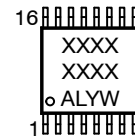CASE 948F
ISSUE B

DATE 19 OCT 2006

16

1

SCALE 2:1

16X K REF

⊕ | 0.10 (0.004) Ⓜ | T U Ⓢ V Ⓢ

△ | 0.15 (0.006) | T U Ⓢ

2X L/2

L

16   9

−U−

B

PIN 1
IDENT.

1   8

A

−V−

△ | 0.15 (0.006) | T U Ⓢ

SECTION N−N

K
K1

J1

J

N

0.25 (0.010)

M

N

F

DETAIL E

C

△ | 0.10 (0.004)

−T− SEATING
PLANE

D   G

H

DETAIL E

−W−
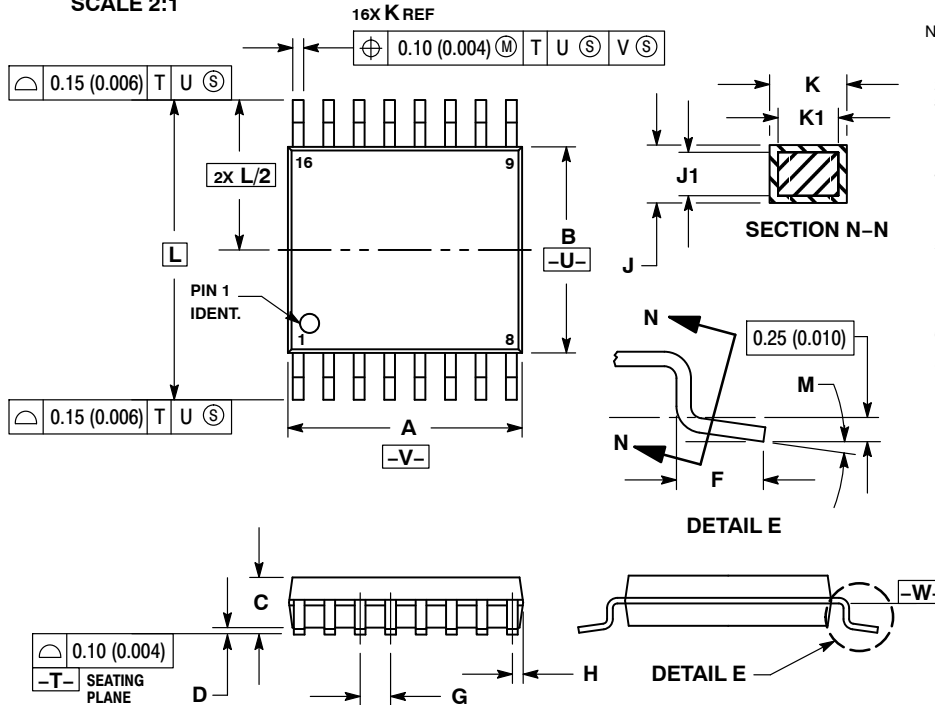
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

**RECOMMENDED
SOLDERING FOOTPRINT***

7.06

1

0.65
PITCH

16X
0.36

16X
1.26

DIMENSIONS: MILLIMETERS
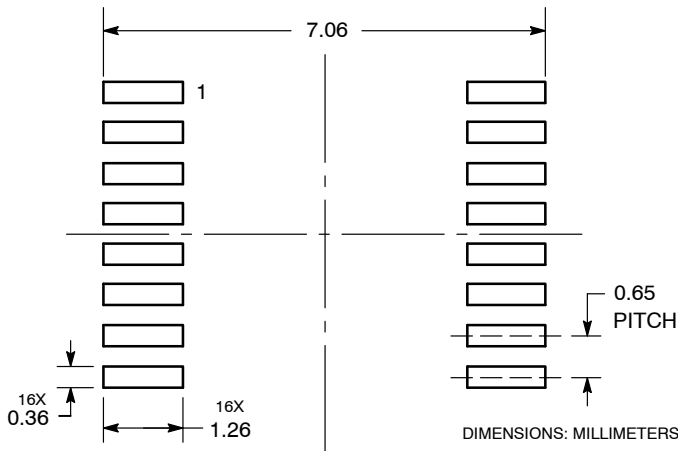
**GENERIC
MARKING DIAGRAM***

16

XXXX
XXXX
◦ ALYW

1

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98ASH70247A	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	TSSOP−16		PAGE 1 OF 1

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical–documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales