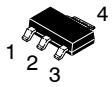
# High Voltage Transistor Surface Mount

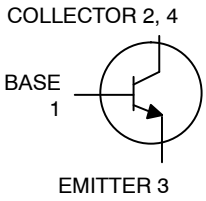
## NPN Silicon

# PZTA42T1G

**SOT−223 PACKAGE**
**NPN SILICON**
**HIGH VOLTAGE TRANSISTOR**
**SURFACE MOUNT**




**SOT−223**
**CASE 318E**
**STYLE 1**




### Features

- PZTA42T1G is Complement to PZTA92T1G
- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

### MAXIMUM RATINGS ($T_C$ = 25°C unless otherwise noted)

| Symbol | Rating | Value | Unit |
|---|---|---|---|
| $V_{CEO}$ | Collector−Emitter Voltage (Open Base) | 300 | Vdc |
| $V_{CBO}$ | Collector−Base Voltage (Open Emitter) | 300 | Vdc |
| $V_{EBO}$ | Emitter−Base Voltage (Open Collector) | 6.0 | Vdc |
| $I_C$ | Collector Current (DC) | 500 | mAdc |
| $P_D$ | Total Power Dissipation @ $T_A$ = 25°C (Note 1) | 1.5 | W |
| $T_{stg}$ | Storage Temperature Range | −65 to +150 | °C |
| $T_J$ | Junction Temperature | 150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

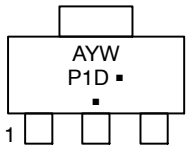
1. Device mounted on a FR−4 glass epoxy printed circuit board 1.575 in x 1.575 in x 0.0625 in; mounting pad for the collector lead = 0.93 sq in.

### THERMAL CHARACTERISTICS

| Symbol | Characteristic | Max | Unit |
|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction−to−Ambient (Note 2) | 83.3 | °C/W |

2. Device mounted on a FR−4 glass epoxy printed circuit board 1.575 in x 1.575 in x 0.0625 in; mounting pad for the collector lead = 0.93 sq in.

### MARKING DIAGRAM




P1D = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| PZTA42T1G | SOT−223 (Pb−Free) | 1,000 / Tape & Reel |
| SPZTA42T1G | SOT−223 (Pb−Free) | 1,000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Symbol | Characteristics | Min | Max | Unit |
|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | |
| $V_{(BR)CEO}$ | Collector-Emitter Breakdown Voltage (Note 3)<br>($I_C$ = 1.0 mAdc, $I_B$ = 0) | 300 | – | Vdc |
| $V_{(BR)CBO}$ | Collector-Base Breakdown Voltage<br>($I_C$ = 100 μAdc, $I_E$ = 0) | 300 | – | Vdc |
| $V_{(BR)EBO}$ | Emitter-Base Breakdown Voltage<br>($I_E$ = 100 μAdc, $I_C$ = 0) | 6.0 | – | Vdc |
| $I_{CBO}$ | Collector-Base Cutoff Current<br>($V_{CB}$ = 200 Vdc, $I_E$ = 0) | – | 0.1 | μAdc |
| $I_{EBO}$ | Emitter-Base Cutoff Current<br>($V_{BE}$ = 6.0 Vdc, $I_C$ = 0) | – | 0.1 | μAdc |
| **ON CHARACTERISTICS** | | | | |
| $h_{FE}$ | DC Current Gain<br>($I_C$ = 1.0 mAdc, $V_{CE}$ = 10 Vdc)<br>($I_C$ = 10 mAdc, $V_{CE}$ = 10 Vdc)<br>($I_C$ = 30 mAdc, $V_{CE}$ = 10 Vdc) | <br>25<br>40<br>40 | <br>–<br>–<br>– | – |
| **DYNAMIC CHARACTERISTICS** | | | | |
| $f_T$ | Current-Gain – Bandwidth Product<br>($I_C$ = 10 mAdc, $V_{CE}$ = 20 Vdc, f = 100 MHz) | 50 | – | MHz |
| $C_{re}$ | Feedback Capacitance<br>($V_{CB}$ = 20 Vdc, $I_E$ = 0, f = 1.0 MHz) | – | 3.0 | pF |
| $V_{CE(sat)}$ | Collector-Emitter Saturation Voltage<br>($I_C$ = 20 mAdc, $I_B$ = 2.0 mAdc) | – | 0.5 | Vdc |
| $V_{BE(sat)}$ | Base-Emitter Saturation Voltage<br>($I_C$ = 20 mAdc, $I_B$ = 2.0 mAdc) | – | 0.9 | Vdc |

3. Pulse Test Conditions, $t_p$ = 300 μs, δ 0.02.

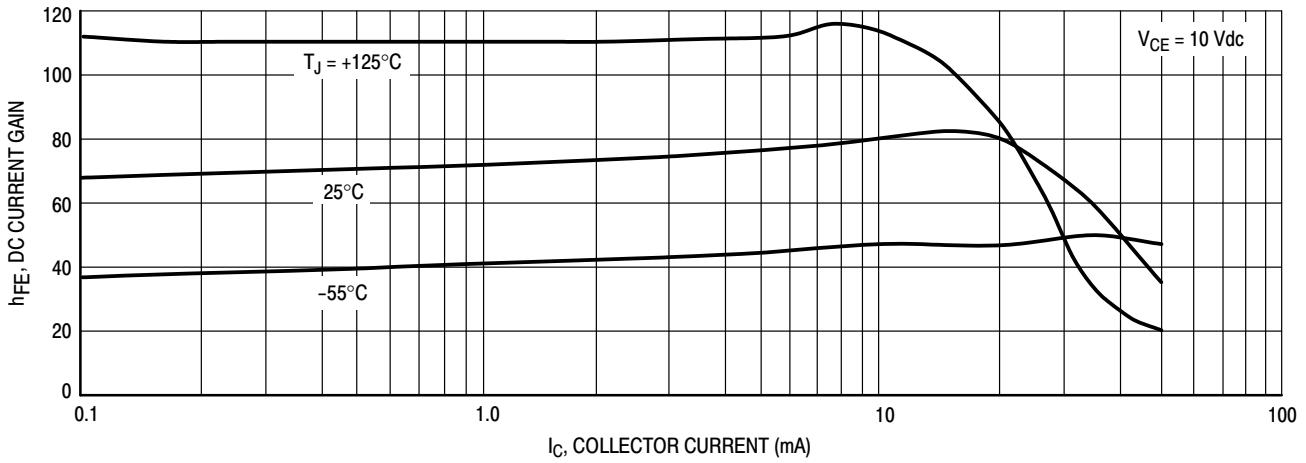


**Figure 1. DC Current Gain**



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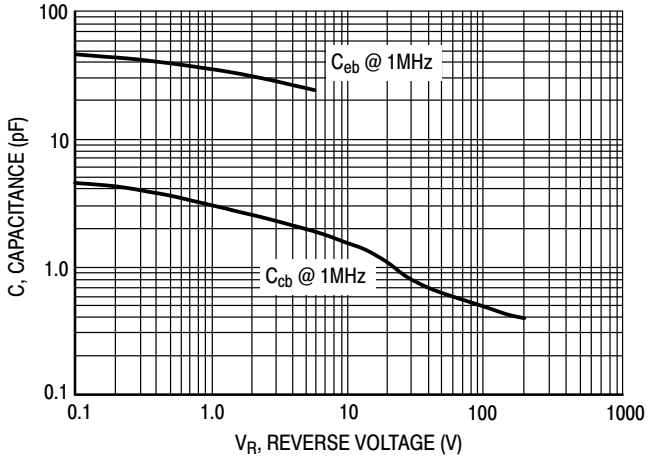


**Figure 2. Capacitance**

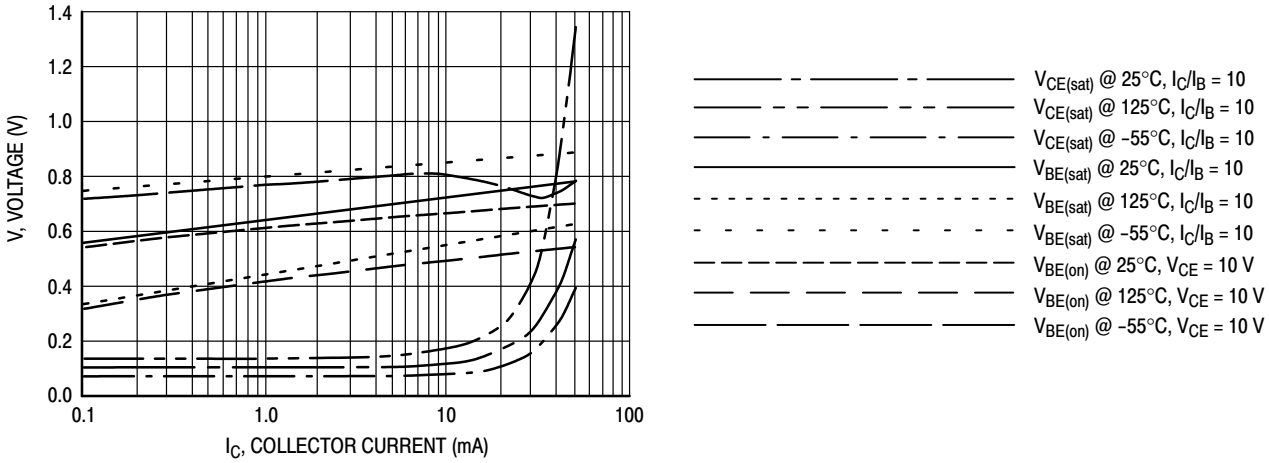


**Figure 3. “ON” Voltages**

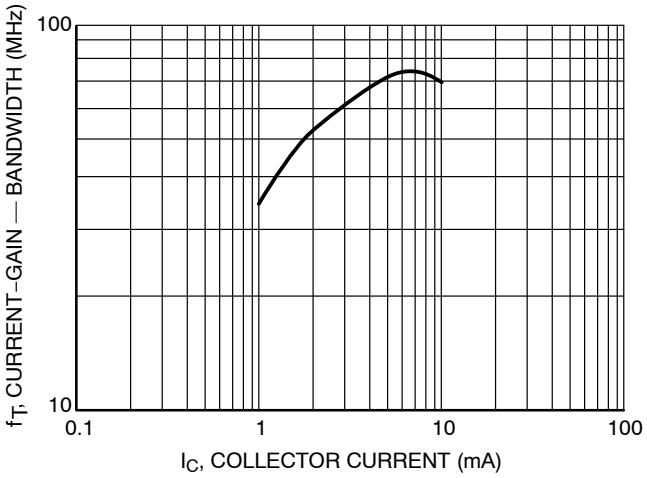


**Figure 4. Current Gain Bandwidth Product**

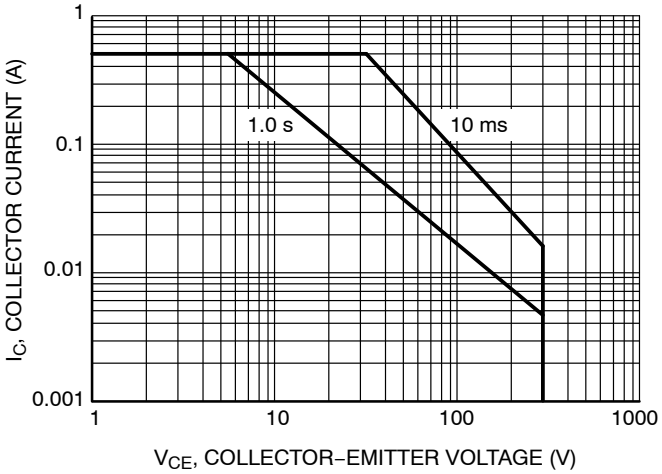


**Figure 5. Safe Operating Area**



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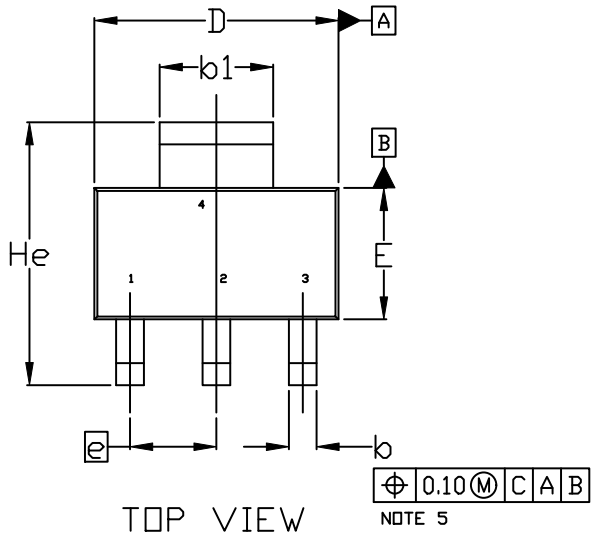
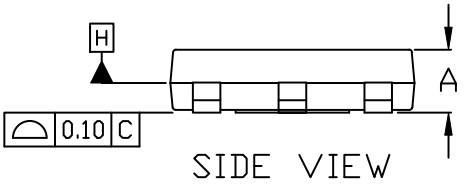
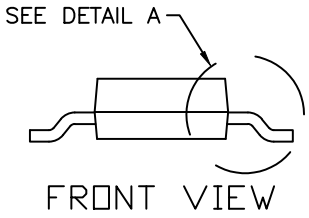
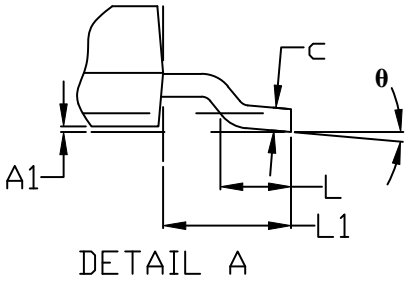
**SOT−223 (TO−261)**
CASE 318E−04
ISSUE R

DATE 02 OCT 2018



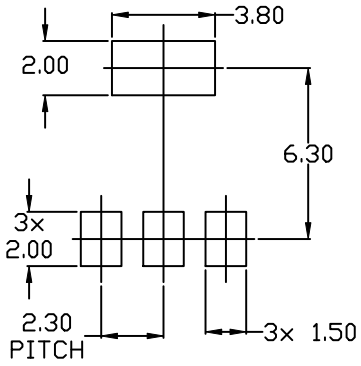




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN. | NOM. | MAX. |
| A | 1.50 | 1.63 | 1.75 |
| A1 | 0.02 | 0.06 | 0.10 |
| b | 0.60 | 0.75 | 0.89 |
| b1 | 2.90 | 3.06 | 3.20 |
| c | 0.24 | 0.29 | 0.35 |
| D | 6.30 | 6.50 | 6.70 |
| E | 3.30 | 3.50 | 3.70 |
| e | 2.30 BSC | | |
| L | 0.20 | --- | --- |
| L1 | 1.50 | 1.75 | 2.00 |
| He | 6.70 | 7.00 | 7.30 |
| θ | 0° | --- | 10° |

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CASE 318E−04
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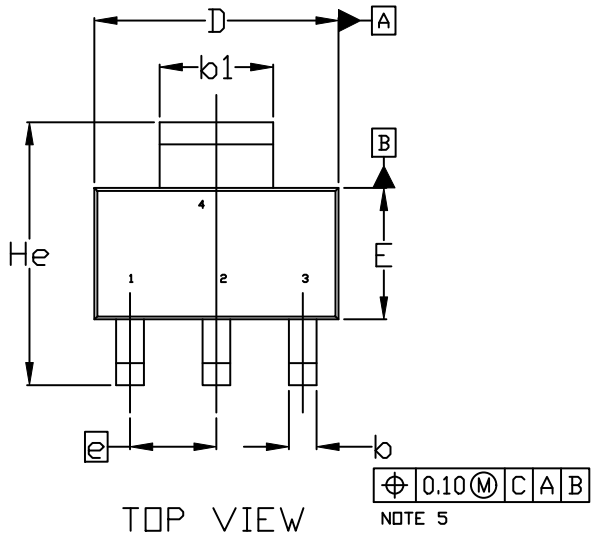


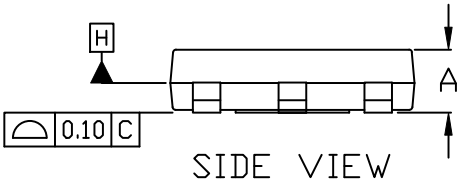


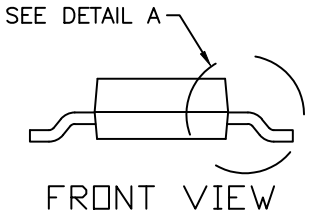


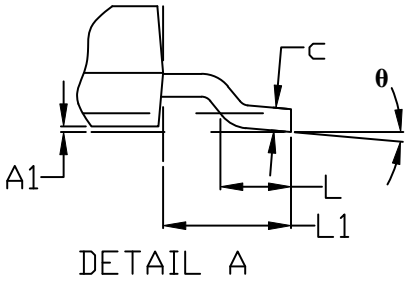


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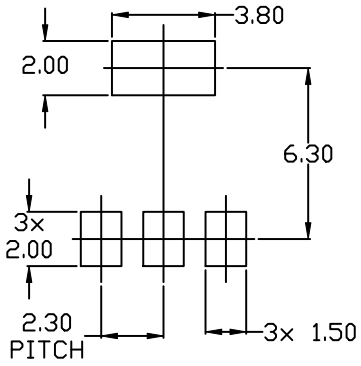
| E | 3.30 | 3.50 | 3.70 |
| e | 2.30 BSC | | |
| L | 0.20 | --- | --- |
| L1 | 1.50 | 1.75 | 2.00 |
| He | 6.70 | 7.00 | 7.30 |
| θ | 0° | --- | 10° |

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**SOT−223 (TO−261)**
CASE 318E−04
ISSUE R

DATE 02 OCT 2018

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

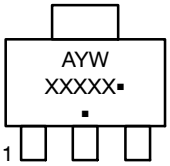
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

## GENERIC MARKING DIAGRAM*




A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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