

SiC JFET Division

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Silicon Carbide (SiC) JFET -EliteSiC, Power N-Channel, D2PAK-7L, 1700 V, 400 mohm

Rev. C, January 2025

Description

UnitedSiC offers the high-performance G3 SiC normally-on JFET transistors. This series exhibits ultra-low on resistance ($R_{DS(ON)}$) and gate charge (Q_{G}) allowing for low conduction and switching loss. The device normally-on characteristics with low $R_{DS(ON)}$ at V_{GS} = 0 V is also ideal for current protection circuits without the need for active control, as well as for cascode operation.

Tab G (1) KS (2) S (3-7)

DATASHEET

F3N170400B7S

Features

- Typical on-resistance $R_{DS(on),typ}$ of $400m\Omega$
- Voltage controlled
- Maximum operating temperature of 175°C
- Extremely fast switching not dependent on temperature
- Low gate charge
- Low intrinsic capacitance
- RoHS compliant
- AECQ Qualified

Typical applications

- Over Current Protection Circuits
- DC-AC Inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating























Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		1700	V
Cata course valtage	V _{GS}	DC	-20 to +3	V
Gate-source voltage	V GS	AC ¹	-30 to +20	V
Continuous drain current ²	ı	T _C = 25°C	6.8	Α
Continuous drain current	I _D	T _C = 100°C	5.1	Α
Pulsed drain current ³	I _{DM}	T _C = 25°C	16	Α
Power dissipation	P _{tot}	T _C = 25°C	68	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T _J ,T _{STG}		-55 to 175	°C
Reflow soldering temperature	T_{solder}	reflow MSL 1	245	°C

- 1. +20V AC rating applies for turn-on pulses <200ns applied with external $R_{G} > 1\Omega$.
- 2. Limited by $T_{\text{\scriptsize J,max}}$
- 3. Pulse width t_p limited by $T_{J,max}$

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
Parameter	Symbol Test Conditions	Min	Тур	Max	Offics	
Thermal resistance, junction-to-case	$R_{ heta$ JC			1.7	2.2	°C/W















Electrical Characteristics ($T_J = +25$ °C unless otherwise specified)

Typical Performance - Static

Parameter	Cumbal	Test Conditions		Value		Units
rai ailletei	Symbol	Test Conditions	Min	Тур	Max	Offics
Drain-source breakdown voltage	BV _{DS}	V_{GS} =-20V, I_D =0.3mA	1700			V
Total duain la cleana augusunt	I_{DSS} $V_{DS}=1700V$,	V _{DS} =1700V, V _{GS} =-20V, T _J =25°C		2.2	60	4
Total drain leakage current		V _{DS} =1700V, V _{GS} =-20V, T _J =175°C		9		μΑ
Tatal asta la cliana sumant		V _{GS} =-20V, T _J =25°C		0.15	6	μА
Total gate leakage current	I _{GSS}	V _{GS} =-20V, T _J =175°C		0.8		μА
		V _{GS} =2V, I _D =5A, T _J =25°C		350		
Drain-source on-resistance	R _{DS(on)}	V _{GS} =0V, I _D =5A, T _J =25°C		400	500	m Ω
Brain source on resistance	(On)	V_{GS} =2V, I_D =5A, T_J =175°C		928		
		V _{GS} =0V, I _D =5A, T _J =175°C		1040		
Gate threshold voltage	V _{G(th)}	V_{DS} =5V, I_D =4.5mA	-11.3	-9	-6.7	V
Gate resistance	R_{G}	f=1MHz, open drain		5		Ω















Typical Performance - Dynamic

Dayamatay	Parameter Symbol Test Conditions		Value			Units	
Parameter	Symbol	rest Conditions	Min	Тур	Max	Units	
Input capacitance	C _{iss}	V _{DS} =100V, V _{GS} =-20V		225			
Output capacitance	C_{oss}	f=100kHz		22		pF	
Reverse transfer capacitance	C_{rss}	1-100KHZ		18			
Effective output capacitance, energy related	C _{oss(er)}	V _{DS} =0V to 1200V, V _{GS} =-20V		11.4		pF	
C _{OSS} stored energy	E_{oss}	V _{DS} =1200V, V _{GS} =-20V		8.2		μJ	
Total gate charge	Q_{G}	V _{DS} =1200V, I _D =5A,		30			
Gate-drain charge	Q_{GD}	$V_{DS} = 1200 \text{ V}, V_{D} = 3 \text{ A},$ $V_{GS} = -18 \text{ V to } 0 \text{ V}$		17		nC	
Gate-source charge	Q_{GS}	VGS - 10V 10 0V		5			
Turn-on delay time	$t_{d(on)}$	V_{DS} =1200V, I_{D} =5A, Gate Driver =-18V to 0V, R_{G} =1 Ω , Inductive Load,		5			
Rise time	t_r			19		ns	
Turn-off delay time	$t_{d(off)}$			9			
Fall time	t_f			37			
Turn-on energy	E _{ON}	FWD: 2x UJ3D1210TS		125		μ	
Turn-off energy	E _{OFF}	in series T _I =25°C		38			
Total switching energy	E_TOTAL	,,		163			
Turn-on delay time	t _{d(on)}			5			
Rise time	t_r	V _{DS} =1200V, I _D =5A, Gate Driver =-18V to 0V,		16		ns	
Turn-off delay time	$t_{d(off)}$	$R_{G}=10,$ $Inductive Load,$ $FWD: 2x UJ3D1210TS$ $in series,$ $T_{J}=150^{\circ}C$		8			
Fall time	t_f			34			
Turn-on energy	E _{ON}			114			
Turn-off energy	E _{OFF}			31		μ	
Total switching energy	E_TOTAL			145			







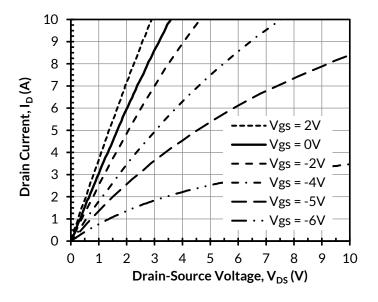








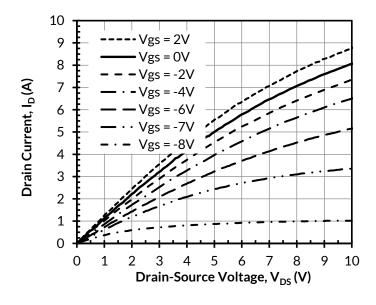
Typical Performance Diagrams



10 9 8 Drain Current, I_D (A) 7 6 -- Vgs = 2V 5 • Vgs = 0V 4 - Vgs = -2V 3 Vgs = -4V2 Vgs = -6V1 Vgs = -7V0 1 2 Drain-Source Voltage, V_{DS} (V)

Figure 1. Typical output characteristics at T_J = - 55°C, tp < 250 μ s

Figure 2. Typical output characteristics at $T_J = 25$ °C, $tp < 250\mu s$



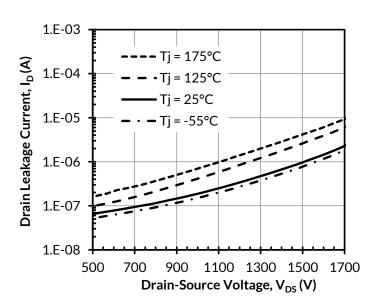


Figure 3. Typical output characteristics at T_J = 175°C, tp < 250 μ s

Figure 4. Typical drain-source leakage at $V_{GS} = -20V$





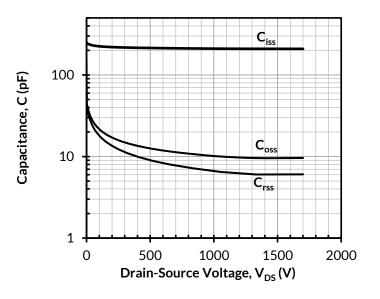












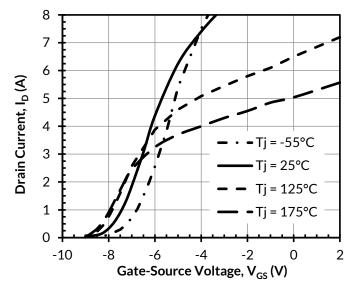
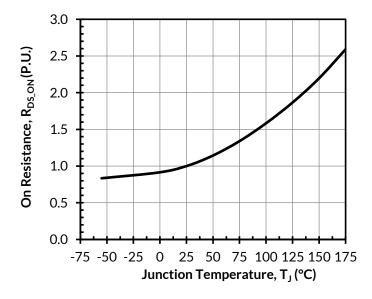


Figure 5. Typical capacitances at f = 100kHz and $V_{GS} = -20V$

Figure 6. Typical transfer characteristics at $V_{DS} = 5V$



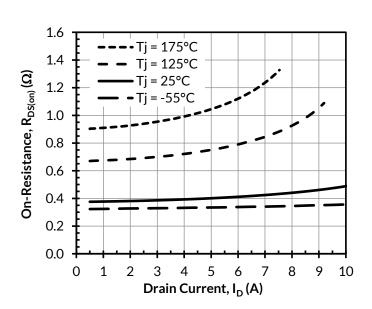


Figure 7. Normalized on-resistance vs. temperature at V_{GS} = 0V and I_D = 5A

Figure 8. Typical drain-source on-resistances at $V_{GS} = 0V$





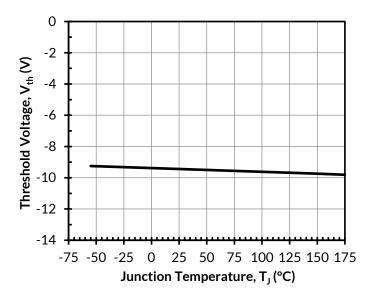








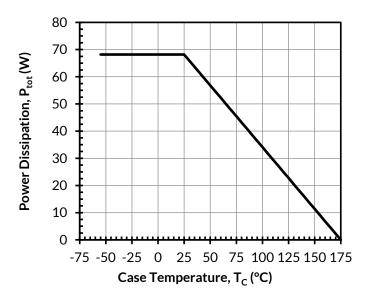




E_{oss}(μJ) Drain-Source Voltage, V_{DS} (V)

Figure 9. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_{D} = 4.5mA

Figure 10. Typical stored energy in C_{OSS} at V_{GS} = -20V



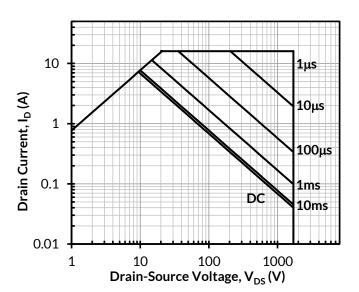


Figure 11. Total power Dissipation

Figure 12. Safe operation area at T_C =25°C, Parameter t_p





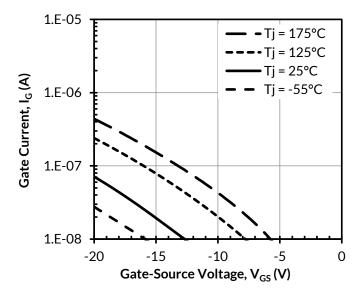








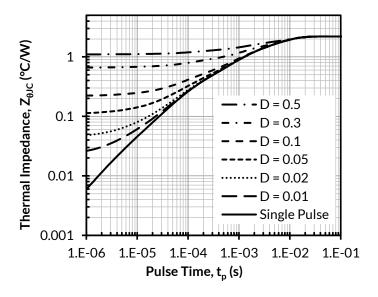




1.0 Tj = 175°C Tj = 125°C 8.0 Gate Current, I_G (A) Tj = 25°C Tj = -55°C 0.6 0.4 0.2 0.0 1 2 0 5 Gate-Source Voltage, $V_{GS}(V)$

Figure 13. Typical gate leakage at $V_{DS} = 0V$

Figure 14. Typical gate forward current at $V_{DS} = 0V$



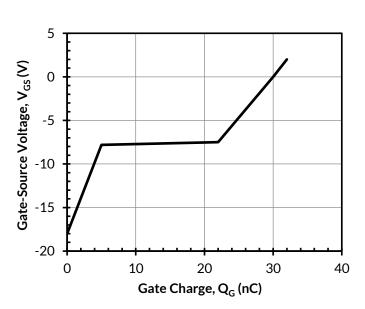


Figure 15. Maximum transient thermal impedance

Figure 16. Typical gate charge at V_{DS} = 1200V and I_{D} = 5A



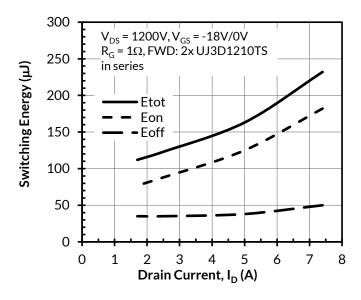












350 Etot 300 Eon Switching Energy (µJ) **Eoff** 250 200 150 $V_{DS} = 1200V, V_{GS} = -18V/0V$ $I_{D} = 5A, T_{J} = 25^{\circ}C$ 100 FWD: 2x UJ3D1210TS in series 50 0 5 10 15 20 0 25 Gate Resistor $R_G(\Omega)$

Figure 17. Clamped inductive switching energy vs. drain current at $T_J = 25$ °C

Figure 18. Clamped inductive switching energy vs. gate resistor R_{G}

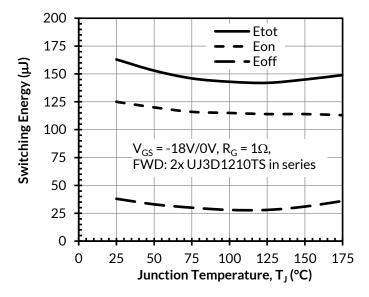


Figure 19. Clamped inductive switching energy vs. junction temperature at V_{DS} = 1200V and I_D = 5A















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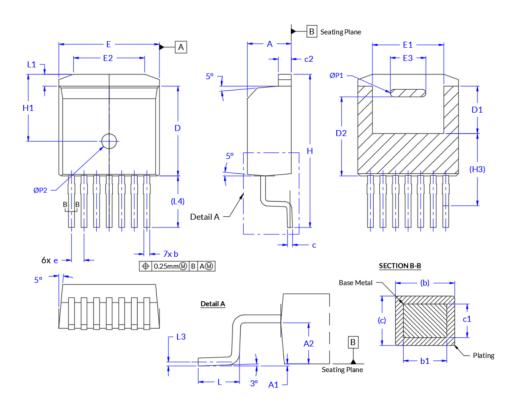
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TO263-7L (D2PAK-7L) PACKAGE OUTLINE, MARKING, TAPE AND REEL SPECIFICATION	PART	Page 1 of 4
DS TO 263 71		Rev D

PACKAGE OUTLINE



	7L-D2PAK				
SYM	М	M	IN	CH	
31141	Min	Max	Min	Max	
Α	4.30	4.56	.169	.180	
A1	0.00	0.25	.000	.010	
A2	2.45	2.75	.096	.108	
b	0.50	0.70	.020	.028	
b1	0.50	-	.020	-	
С	0.40	0.60	.016	.024	
c1	0.40		.016		
c2	1.20	1.40	.047	.055	
D	8.93	9.23	.352	.363	
D1	4.65	4.95	.183	.195	
D2	7.90	8.10	.311	.319	
e	1.27	BSC	.050	BSC	
E	10.08	10.28	.397	.405	
E1	6.82	7.62	.269	.300	
E2	6.50	8.60	.256	.339	
E3	3.50	3.70	.138	.146	
Н	15.00	16.00	.591	.630	
H1	6.68	6.88	.263	.271	
H3	7.31	REF.	.287	REF	
L	1.90	2.50	.075	.098	
L1	0.98	1.42	.039	.056	
L3	0.25	BSC	.0098	BSC	
L4	5.22	REF	.205	REF	
ØP1	0.65	0.85	.026	.033	
ØP2	1.40	1.60	.055	.063	

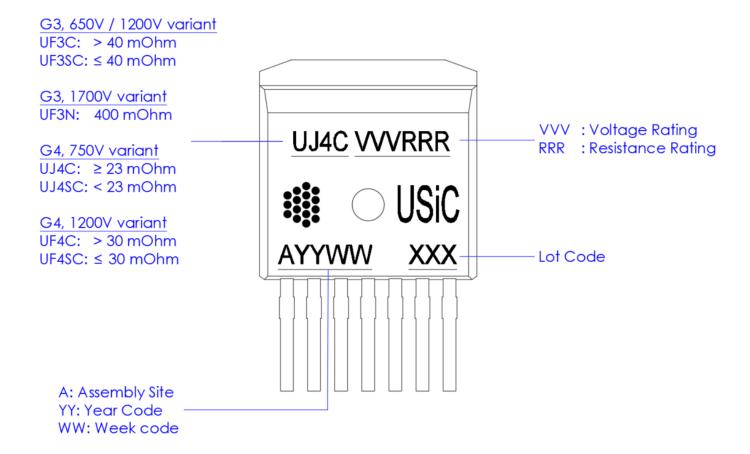
Notes:

- 1. GENERAL TOLERANCE: ±0.1 unless otherwise specified
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. PACKAGE BODY SIDES EXCLUDE MOLD FLASH AND GATE BURRS.
- 4. DIMENSION LIS MEASURED IN GAUGE LINE.
- 5. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
- 6. DIMENSION c1 AND b1 APPLIES TO BASE METAL ONLY



TO263-7L (D2PAK-7L) PACKAGE OUTLINE, PART MARKING, TAPE AND REEL SPECIFICATION	Page 2 of 4
DS_TO_263_7L	Rev D

PART MARKING



Template: FOR-000530 Rev G



TO263-7L	(D2PAK-7L)	PACKAGE	OUTLINE,	PART
MARKING,	TAPE AND RE	EL SPECIFIC	ATION	

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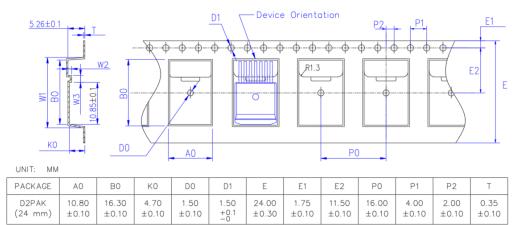
Page **3** of **4**

Rev D

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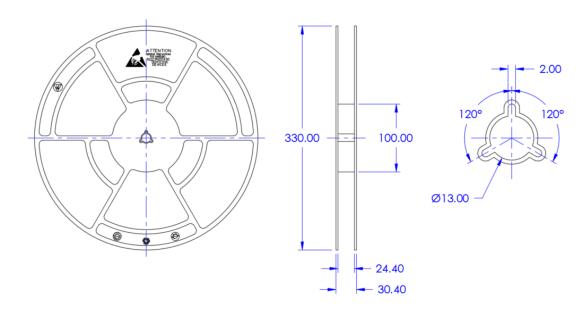
PACKING TYPE

Carrier Tape



Ext	erior	size	
	W1	16.9±0.1	
Spec	W2	1.3±0.1	
'	W3	1.0±0.1	
	W1	17.2±0.1	(1)
Spec 2	W2	1.8±0.1	(b)
	W3	0.85±0.1	0

Reel



All dimensions in millimeters Anti-Static Tape and Rell (T&R) Quantity per Reel: 800 units



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REVISION HISTORY

Revision	Create Date (mm/dd/yyyy)	Description of Change	Initiator of Change
С	11/06/2023	Updated to Qorvo template Updated Package outline drawing based latest drawing revision	Glenn Galang
D	05/21/2024	Added illustration of device orientation on carrier tape (page 3)	Glenn Galang

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