SiC JFET Division

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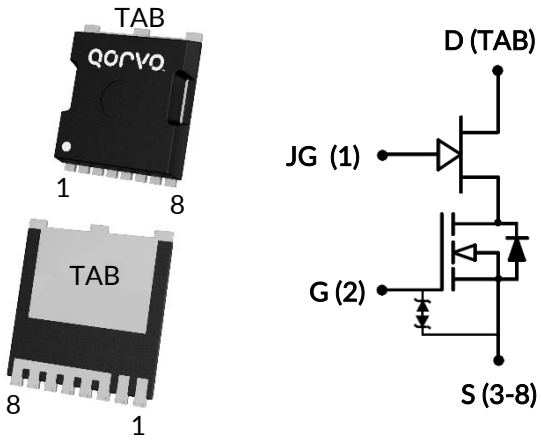
DATASHEET

UG4SC075005L8S



Part Number	Package	Marking
UG4SC075005L8S	MO-229	UG4SC075005

RoHS COMPLIANT | Pb LEAD FREE | HF HALOGEN FREE

Silicon Carbide (SiC) Combo JFET - EliteSiC, Power N-Channel, TOLL, 750 V, 5 mohm

Preliminary, January 2025

Description

Qorvo's UG4SC075005L8S "Combo-FET" integrates both a 750V SiC JFET and a Low Voltage Si MOSFET into a single TOLL package. This innovative approach allows users to create circuitry that would enable a normally-off switch while leveraging the benefits of a normally-on SiC JFET. These benefits include ultra-low on-resistance ($R_{DS(on)}$) to minimize conduction losses and the exceptional robustness characteristic of a simplified JFET device structure, making it capable of handling the high-energy switching required in circuit protection applications. For switch-mode power conversion application, this device provides separate access to the JFET and MOSFET gates for improved speed control and ease of paralleling multiple devices.

Features

- Single digit $R_{DS(on)}$
- Normally-off capability
- Improved speed control
- Improved parallel device operation (3+ FETs)
- Operating temperature: 175°C (max)
- High pulse current capability
- Excellent device robustness
- Silver-sintered die attach for excellent thermal resistance
- Short circuit rated

Typical applications

- Solid State / Semiconductor Circuit Breaker
- Solid State / Semiconductor Relay
- Battery Disconnects
- Surge Protection
- Inrush Current Control
- High power switch mode converters (>25kW)

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		750	V
JFET Gate (JG) to source voltage	V_{JGS}	DC	-30 to +3	V
		AC [1]	-30 to +30	V
MOSFET Gate (G) to source voltage	V_{GS}	DC	-20 to +20	V
		AC (f > 1Hz)	-25 to +25	V
Continuous drain current [2]	I_D	T_C < 144°C	120	A
Pulsed drain current [3]	I_{DM}	T_C = 25°C	588	A
Single pulsed avalanche energy [4]	E_{AS}	L=15mH, I_{AS} = 6.5A	316	mJ
Power dissipation	P_{tot}	T_C = 25°C	1153	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T_J,T_{STG}		-55 to 175	°C
Reflow soldering temperature	T_{solder}	reflow MSL 1	260	°C

1. +30V AC rating applies for turn-on pulses <200ns applied with external R_G > 1Ω.
2. Limited by bondwires
3. Pulse width t_p limited by $T_{J,max}$
4. Starting T_J = 25°C

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.10	0.13	°C/W

Electrical Characteristics (T_J = +25°C and V_{JGS} = 0V unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	V_{GS}=0V, I_D=1mA	750			V
Total drain leakage current	I_{DSS}	V_{DS}=750V, V_{GS}=0V, T_J=25°C		6	130	µA
		V_{DS}=750V, V_{GS}=0V, T_J=175°C		45		
Total JFET gate leakage current	I_{JGSS}	V_{GS}=-20V, V_{GS}=12V		0.1	100	µA
Total MOSFET gate leakage current	I_{GSS}	V_{GS}=-20V / +20V		6	20	µA
Drain-source on-resistance	$R_{DS(on)}$	V_{GS}=15V, V_{JGS}=2V, I_D=80A, T_J=25°C		5.0		mΩ
		V_{GS}=15V, V_{JGS}=0V, I_D=80A, T_J=25°C		5.4	7.2	
		V_{GS}=15V, V_{JGS}=0V, I_D=80A, T_J=125°C		9.3		
		V_{GS}=15V, V_{JGS}=0V, I_D=80A, T_J=175°C		12.2		
JFET gate threshold voltage	$V_{JG(th)}$	V_{DS}=5V, V_{GS}=12V, I_D=180mA	-8.3	-6.0	-3.7	V
MOSFET gate threshold voltage	$V_{G(th)}$	V_{DS}=5V, I_D=10mA	4	4.7	6	V
JFET gate resistance	R_{JG}	f=1MHz, open drain		0.8		Ω
MOSFET gate resistance	R_G	f=1MHz, open drain		0.8		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current [1]	I_S	T_C < 144°C			120	A
Diode pulse current [2]	$I_{S,pulse}$	T_C = 25°C			588	A
Forward voltage	V_{FSD}	V_{GS}=0V, I_S=50A, T_J=25°C		1.03	1.16	V
		V_{GS}=0V, I_S=50A, T_J=175°C		1.06		
Reverse recovery charge	Q_{rr}	V_{DS}=400V, I_S=80A, V_{GS}=0V, V_{JGS}=0V, R_{JG}=0.7Ω, di/dt=2400A/µs, T_J=25°C		377		nC
Reverse recovery time	t_{rr}			70		ns
Reverse recovery charge	Q_{rr}	V_{DS}=400V, I_S=80A, V_{GS}=0V, V_{JGS}=0V, R_{JG}=0.7Ω, di/dt=2400A/µs, T_J=150°C		427		nC
Reverse recovery time	t_{rr}			78		ns

Typical Performance - Dynamic with MOSFET gate as control terminal and V_{JGS}=0V

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
MOSFET input capacitance	C_{iss}	V_{DS}=400V, V_{GS}=0V, f=100kHz		8374		pF
Output capacitance	C_{oss}			362		
Reverse transfer capacitance	C_{rss}			4		
Effective output capacitance, energy related	$C_{oss(er)}$	V_{DS}=0V to 400V, V_{GS}=0V		475		pF
Effective output capacitance, time related	$C_{oss(tr)}$			950		pF
Total Gate charge	Q_G	V_{DS}=400V, I_D=80A, V_{GS} = 0V to 15V		164		nC
Gate-drain charge	Q_{GD}			24		
Gate-source charge	Q_{GS}			46		

Typical Performance - Dynamic with JFET gate as control terminal and V_{GS}=+12V

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
JFET input capacitance	C_{Jiss}	V_{DS}=400V, V_{JGS}=-20V, f=100kHz		3028		pF
JFET output capacitance	C_{Joss}			364		
JFET reverse transfer capacitance	C_{Jrss}			360		
JFET total gate charge	Q_{JG}	V_{DS}=400V, I_D=80A, V_{JGS} = -18V to 0V		400		nC
JFET gate-drain charge	Q_{JGD}			270		
JFET gate-source charge	Q_{JGS}			60		

Typical Performance Diagrams - MOSFET gate as control terminal and V_{JGS}=0V

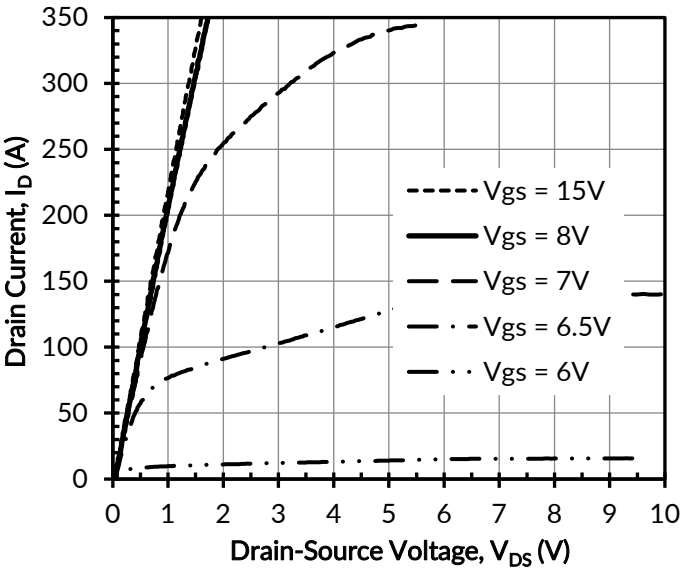


Figure 1. Typical output characteristics at T_J = - 55°C, tp < 250µs

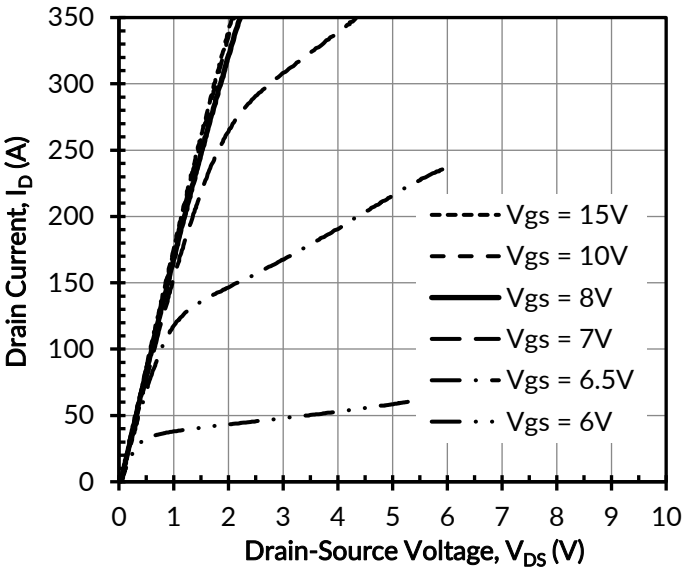


Figure 2. Typical output characteristics at T_J = 25°C, tp < 250µs

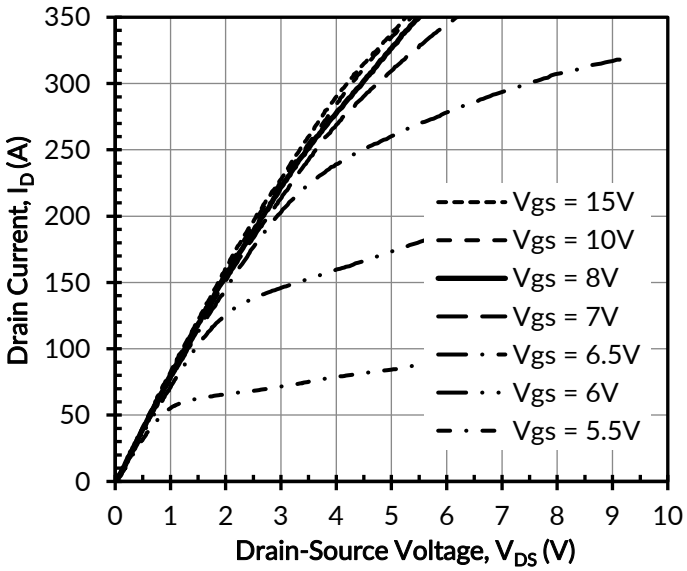


Figure 3. Typical output characteristics at T_J = 175°C, tp < 250µs

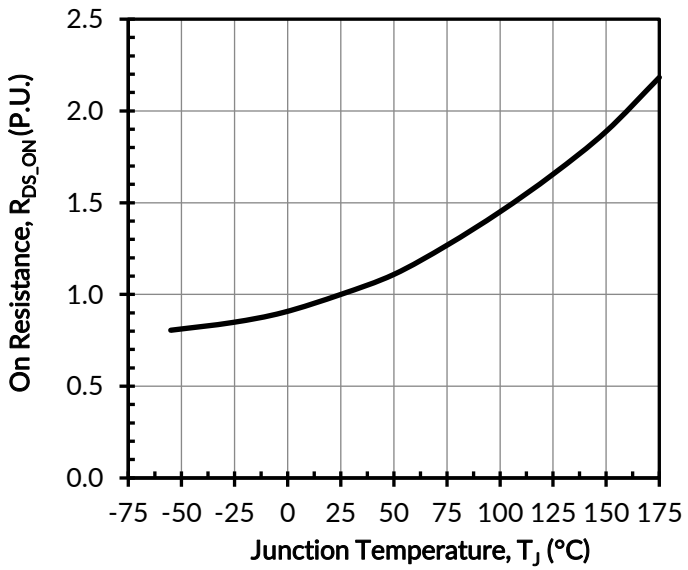


Figure 4. Normalized on-resistance vs. temperature at V_{GS} = 12V and I_D = 80A

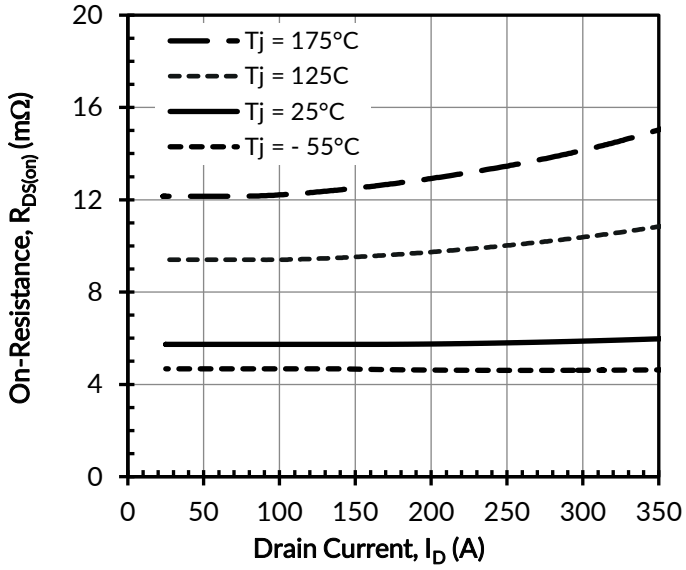


Figure 5. Typical drain-source on-resistances at V_{GS} = 12V

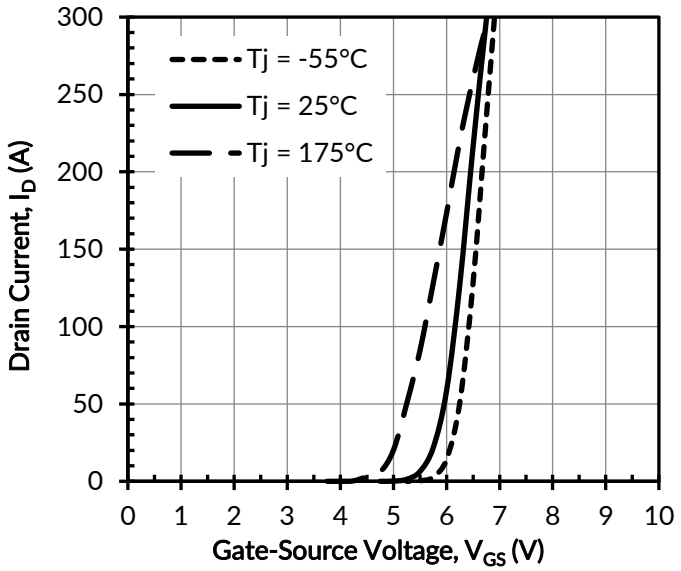


Figure 6. Typical transfer characteristics at V_{DS} = 5V

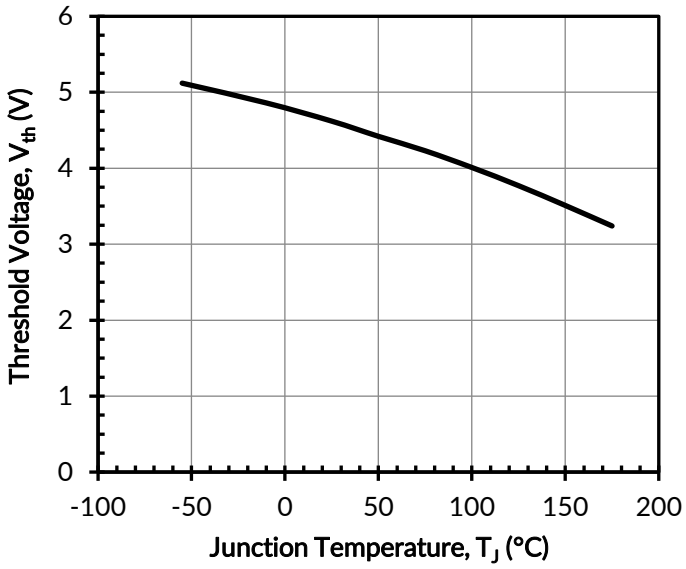


Figure 7. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_D = 10mA

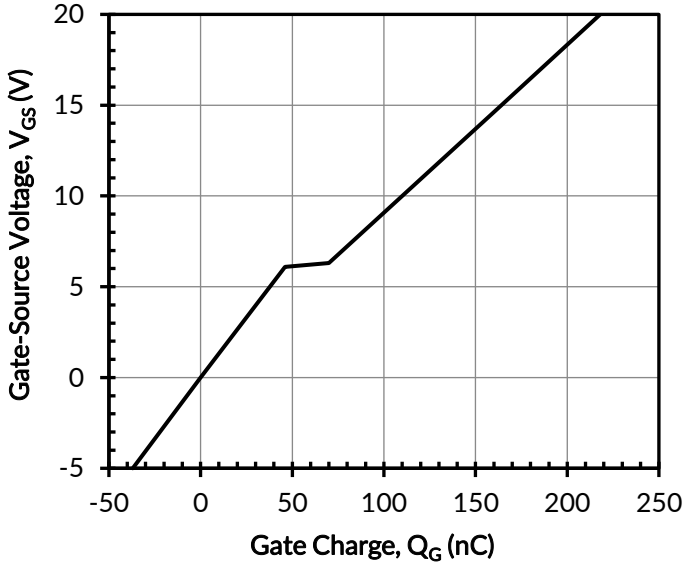


Figure 8. Typical gate charge at V_{DS} = 400V and I_D = 80A

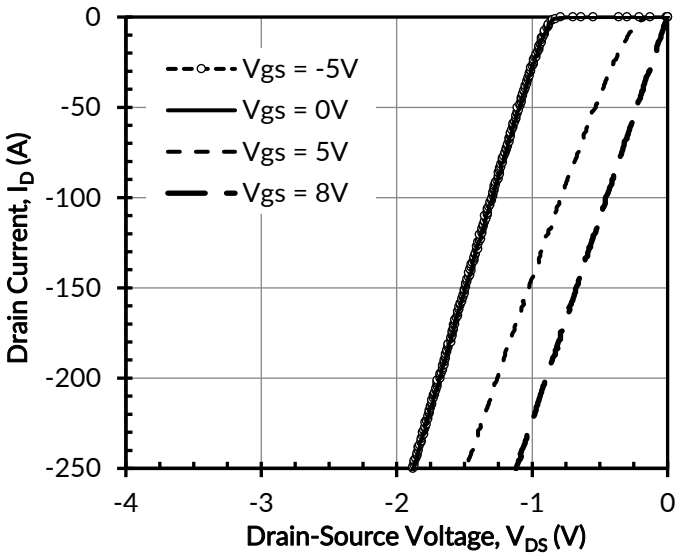


Figure 9. 3rd quadrant characteristics at T_J = -55°C

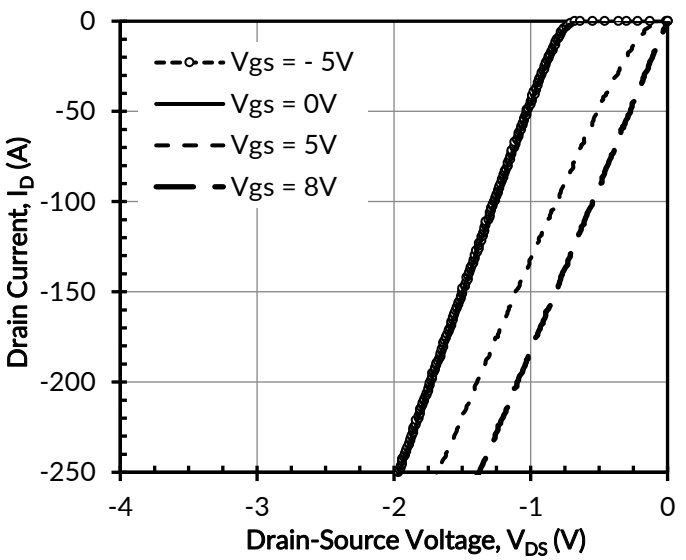


Figure 10. 3rd quadrant characteristics at T_J = 25°C

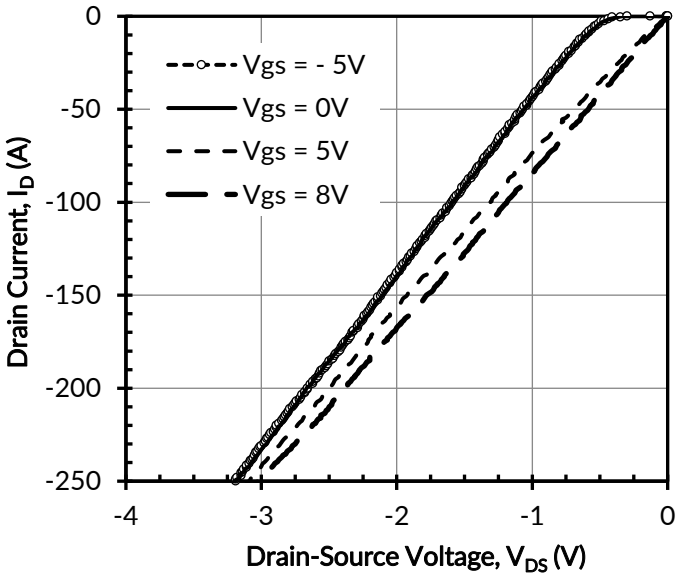


Figure 11. 3rd quadrant characteristics at T_J = 175°C

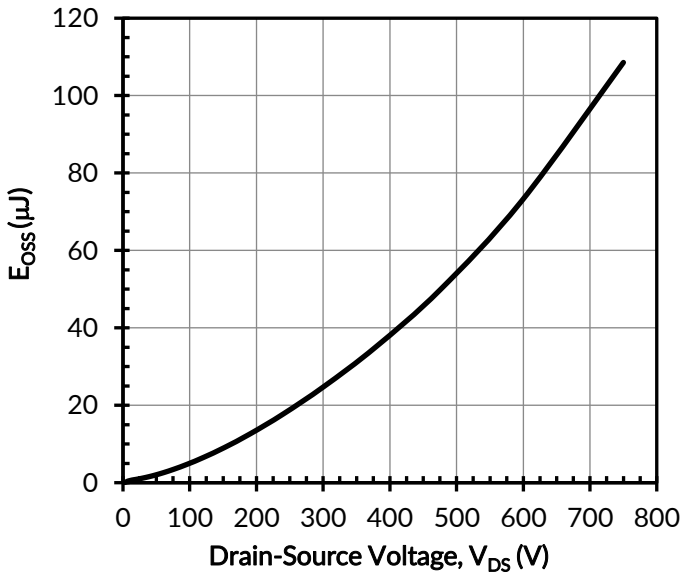


Figure 12. Typical stored energy in C_{OSS} at V_{GS} = 0V

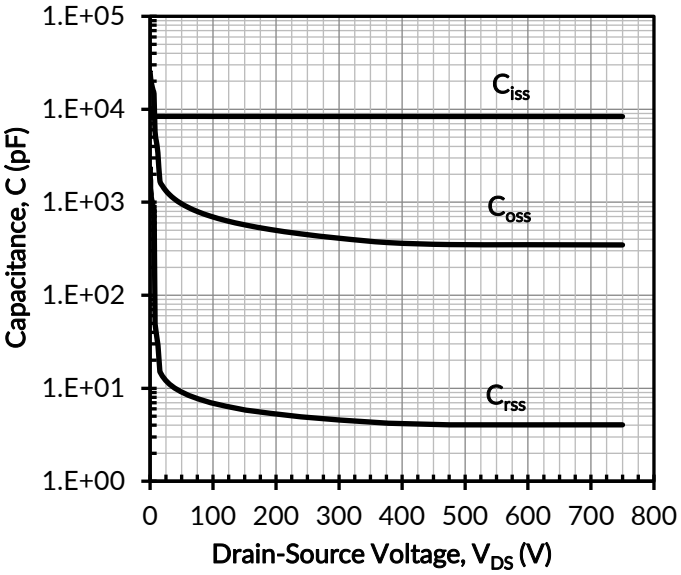


Figure 13. Typical capacitances at f = 100kHz and V_{GS} = 0V

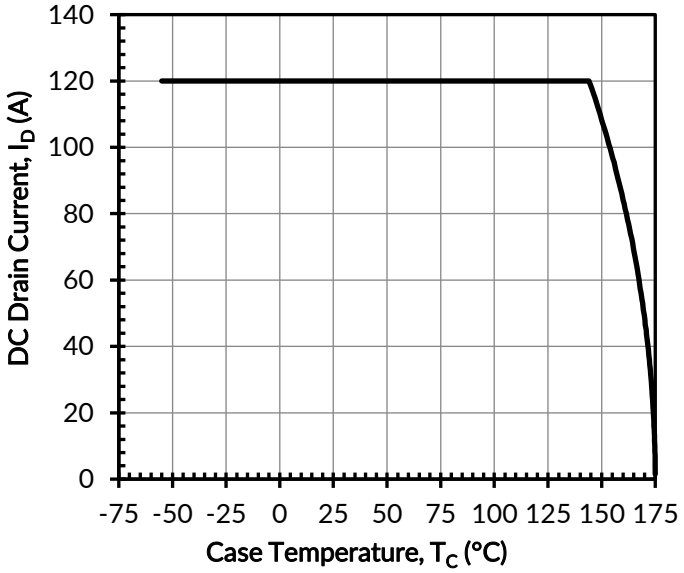


Figure 14. DC drain current derating

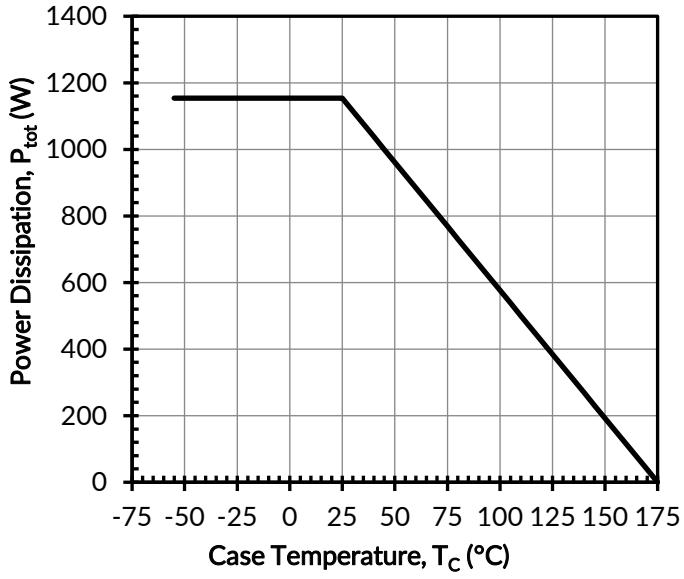
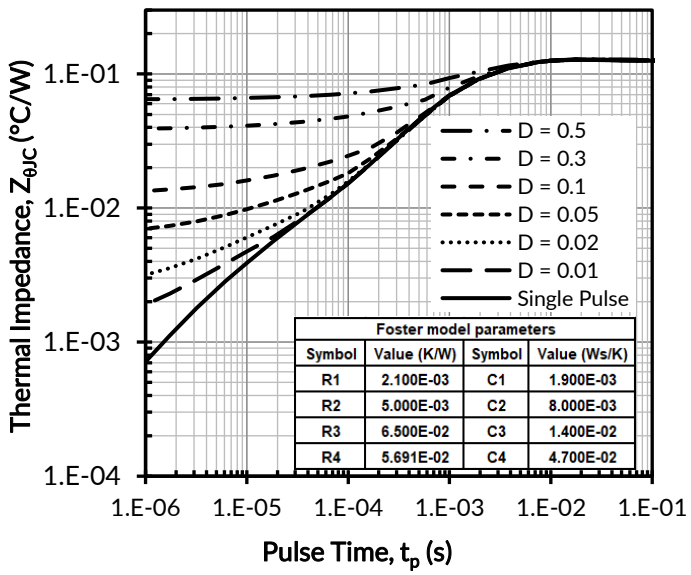


Figure 15. Total power dissipation



Foster model parameters

Symbol	Value (K/W)	Symbol	Value (Ws/K)
R1	2.100E-03	C1	1.900E-03
R2	5.000E-03	C2	8.000E-03
R3	6.500E-02	C3	1.400E-02
R4	5.691E-02	C4	4.700E-02

Figure 16. Maximum transient thermal impedance

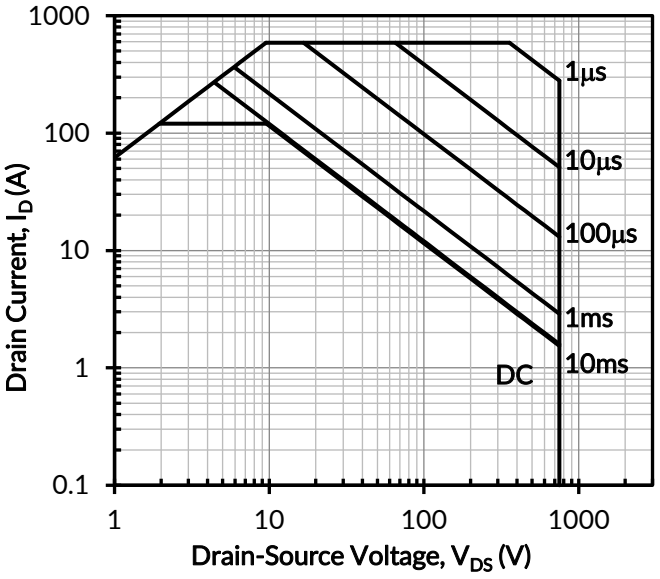


Figure 17. Safe operation area at T_C = 25°C, D = 0, Parameter t_p

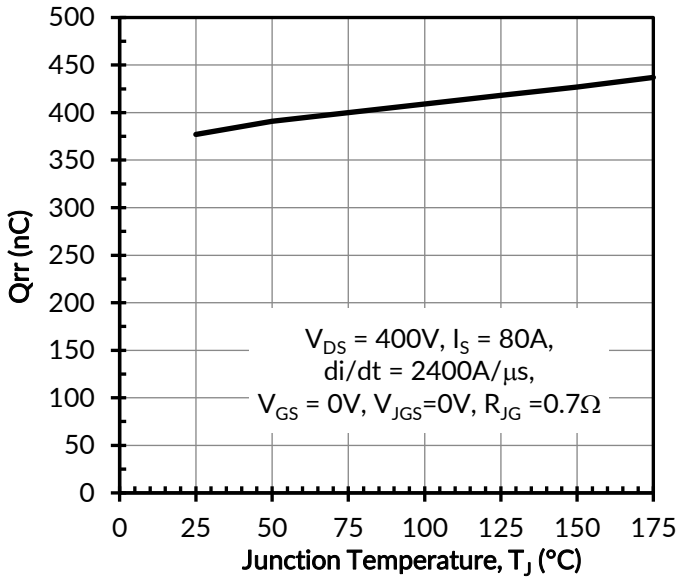


Figure 18. Reverse recovery charge Qrr vs. junction temperature

Typical Performance Diagrams - JFET gate as control terminal and V_{GS}=+12V

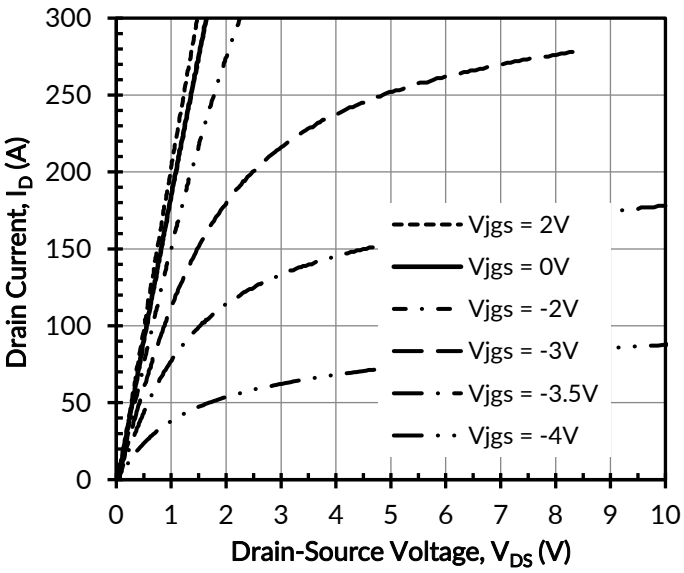


Figure 19. Typical output characteristics with JFET gate as control at T_J = - 55°C, t_p < 250µs

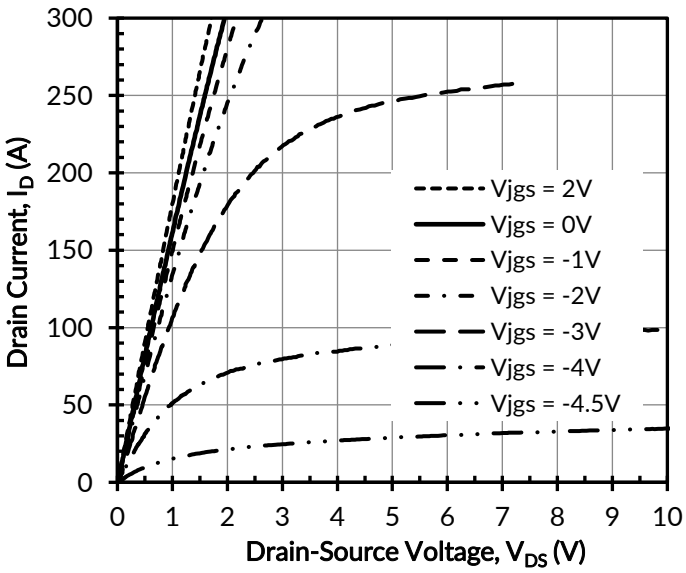


Figure 20. Typical output characteristics with JFET gate as control at T_J = 25°C, t_p < 250µs

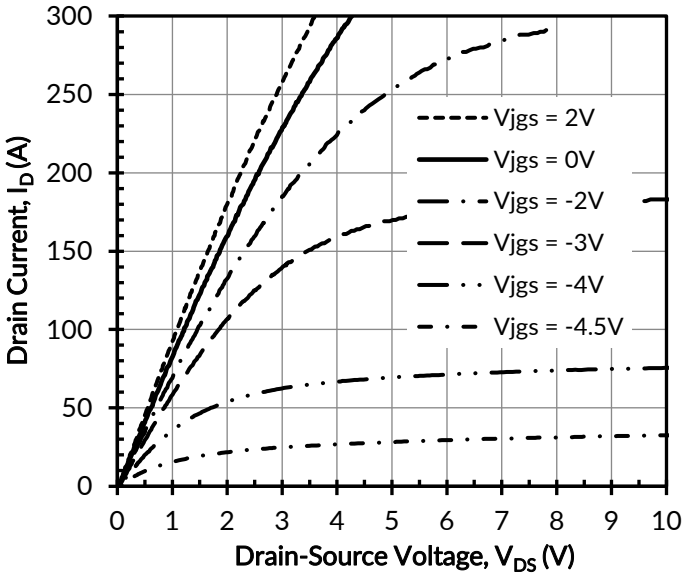


Figure 21. Typical output characteristics with JFET gate as control at T_J = 175°C, t_p < 250µs

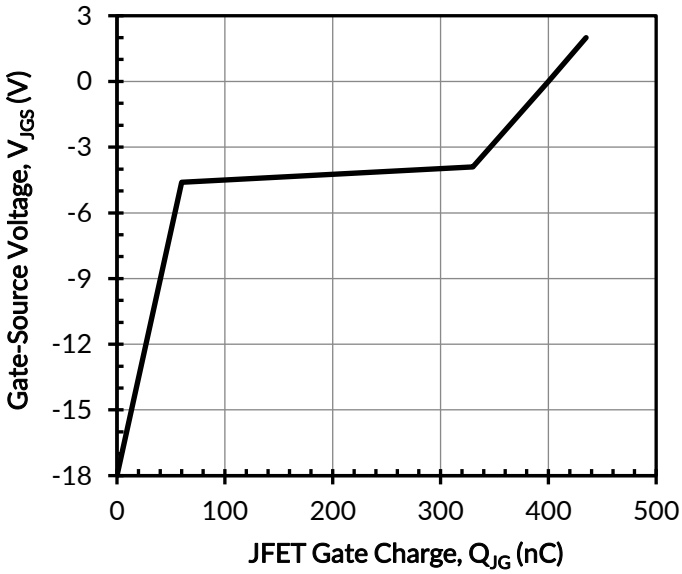


Figure 22. Typical JFET gate charge at V_{DS} = 400V and I_D = 80A

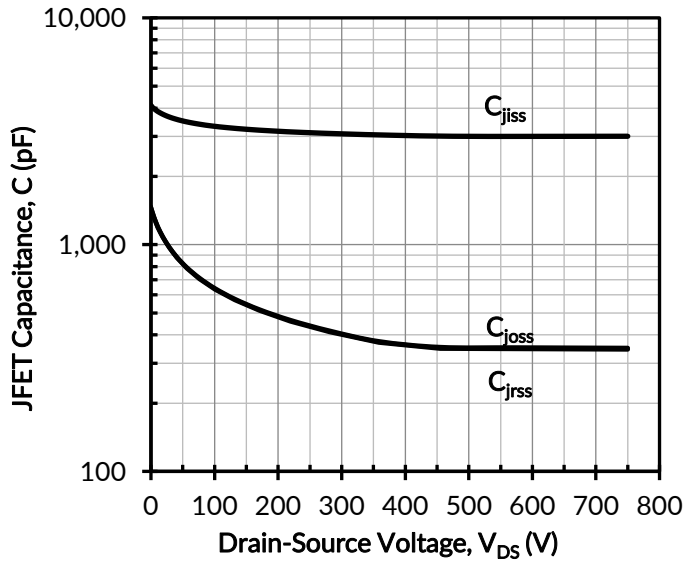
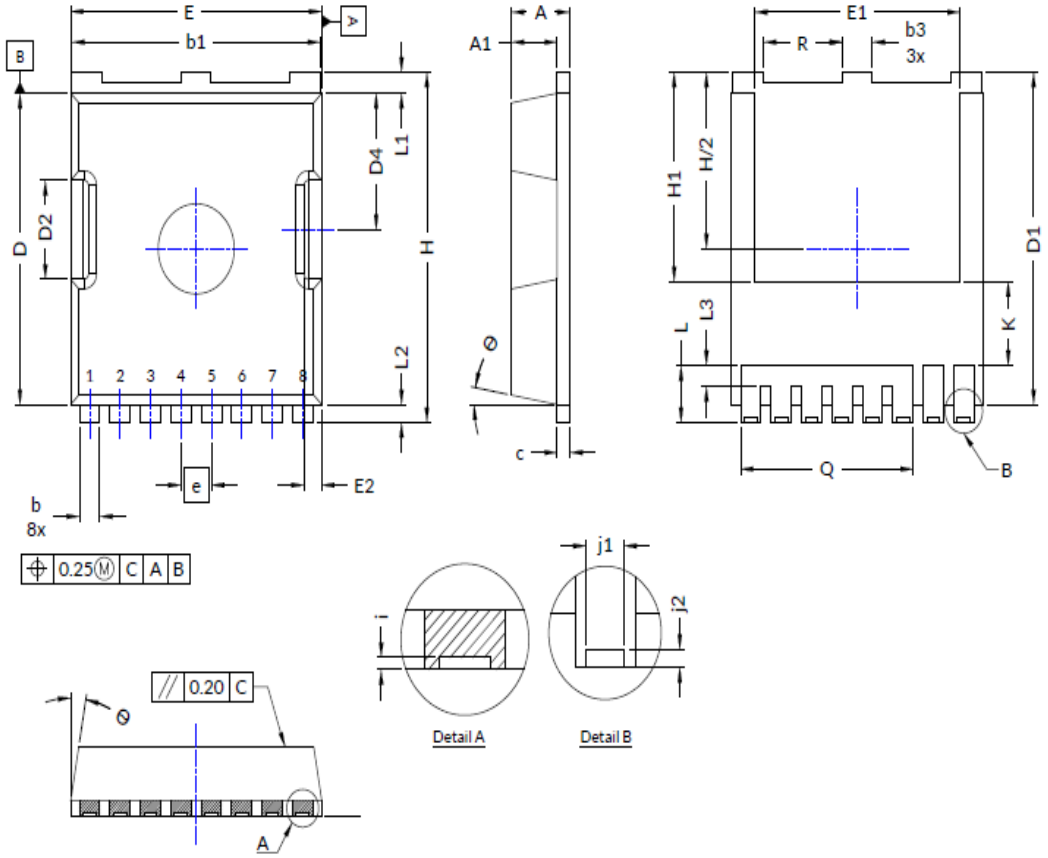


Figure 23. Typical JFET capacitances at f = 100kHz and V_{JGS} = -20V

Package Outlines



SYMBOL	TO-LL		
	Value		
	Min	Nom	Max
A	2.15	2.30	2.45
A1		1.80 REF	
b	0.70	0.80	0.90
b1	9.65	9.80	9.95
b3	1.10	1.20	1.30
c	0.40	0.50	0.60
D	10.18	10.38	10.58
D1	10.98	11.08	11.18
D2	3.15	3.30	3.45
D4	4.40	4.55	4.70
E	9.70	9.90	10.10
E1	7.95	8.10	8.25
E2	0.60	0.70	0.80
e		1.20 BSC	
H	11.48	11.68	11.88
H1	6.80	6.95	7.10
i		0.10 REF	
j1		0.46 REF	
j2		0.20 REF	
K		2.80 REF	
L	1.40	1.90	2.10
L1	0.50	0.70	0.90
L2	0.48	0.60	0.72
L3	0.30	0.70	0.80
Q		6.80 REF	
R	3.00	3.10	3.20
θ		10°	

Note:
1. All dimensions in millimeters
2. Dimensions does not include Burrs and Mold Flashes
3. Dimensions in compliance with JEDEC MO-299B except for backside heatsink exposed pad dimension, E1 and H1

Pin Designations:
1 : Gate
2 : Source Kelvin
3-8 : Source

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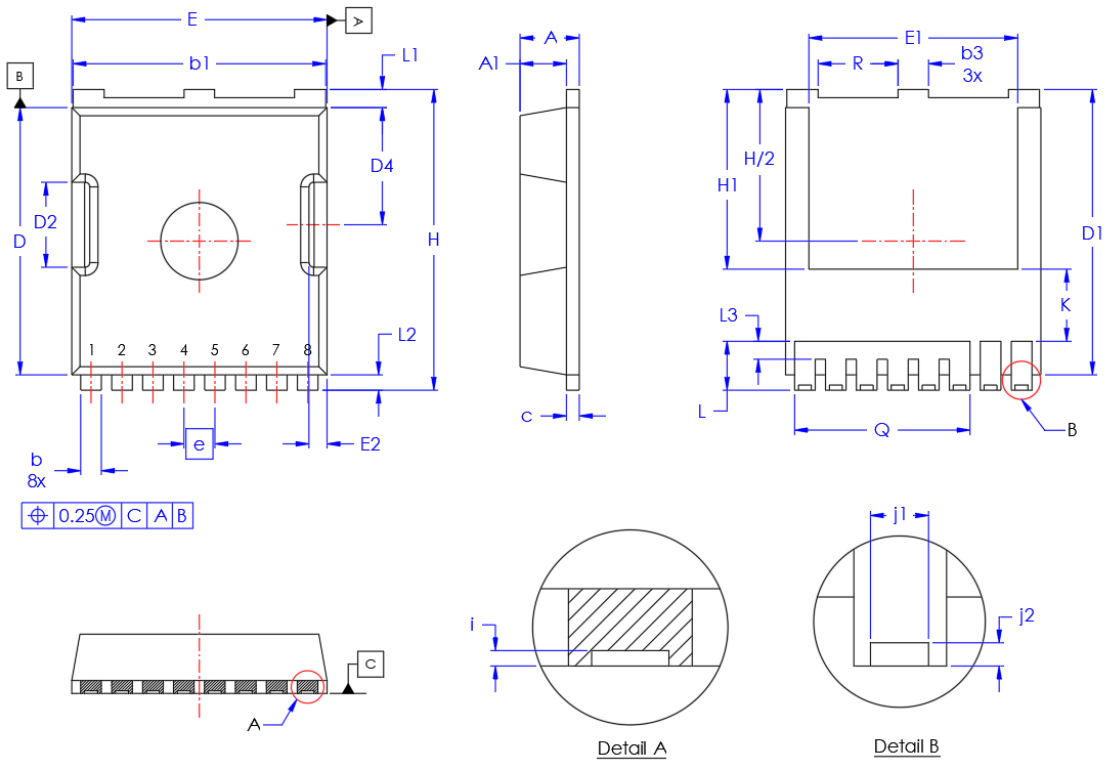
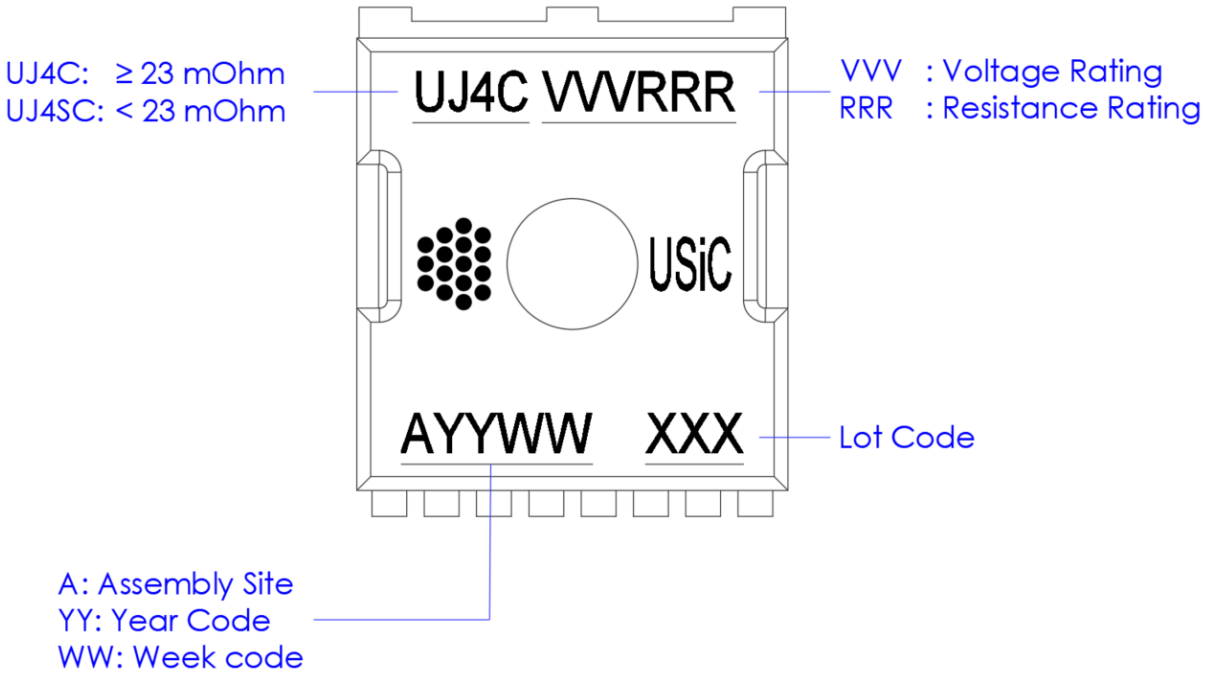
PACKAGE OUTLINE



SYMBOL	TO-LL Value	
	Min	Max
A	2.15	2.45
A1	1.80 REF	
b	0.65	0.90
b1	9.65	9.95
b3	1.10	1.30
c	0.40	0.60
D	10.18	10.58
D1	10.88	11.28
D2	3.15	3.45
D4	4.40	4.70
E	9.70	10.10
E1	7.95	8.25
E2	0.60	0.80
e	1.20 BSC	
H	11.48	11.88
H1	6.80	7.10
i	0.10 REF	
j1	0.46 REF	
j2	0.20 REF	
K	2.80 REF	
L	1.40	2.10
L1	0.50	0.90
L2	0.48	0.72
L3	0.30	0.80
Q	6.80 REF	
R	3.00	3.20

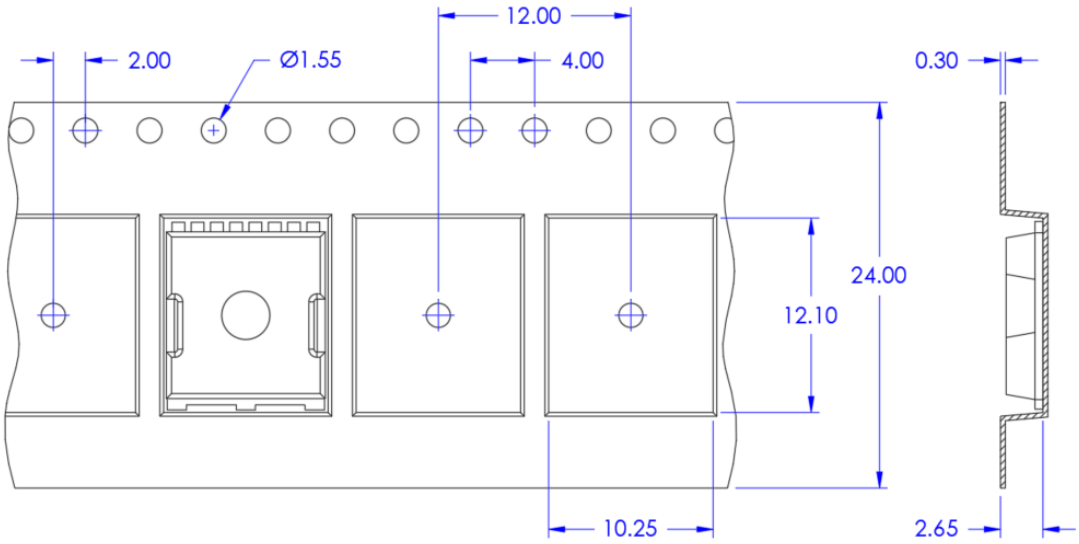
Note:
1. All dimensions in millimeters
2. Dimensions does not include Burrs and Mold Flashes

PART MARKING

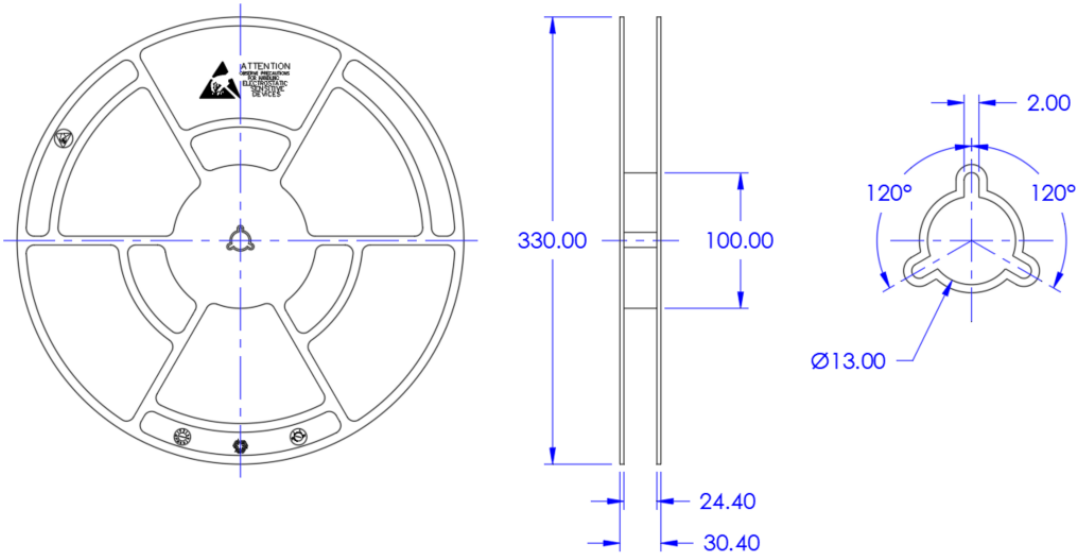


PACKING TYPE

Carrier Tape



Reel



All dimensions in millimeters
Quantity per Reel: 2000 units

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REVISION HISTORY

Revision	Create Date (mm/dd/yyyy)	Description of Change	Initiator of Change
A	10/13/2023	Initial Production Release	Glenn Galang
B	01/31/2024	Corrected device orientation inside carrier tape pocket (Page 3)	Glenn Galang

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
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