SiC JFET Division

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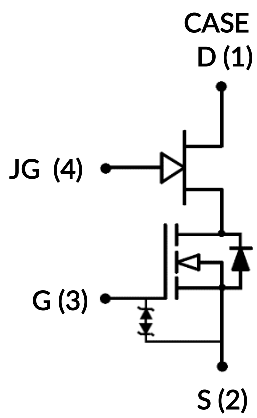
Silicon Carbide (SiC) Combo JFET - EliteSiC, Power N-Channel, TO-247-4L, 750 V, 10 mohm

(SiC JFET w/ Si MOSFET)

DATASHEET

UG4SC075011K4S

Rev. C, January 2025



Part Number	Package	Marking
UG4SC075011K4S	TO-247-4L	UG4SC075011K4S

RoHS COMPLIANT · Pb LEAD FREE · HF HALOGEN FREE

Description

Qorvo's UG4SC075011K4S "Combo-FET" integrates both a 750V SiC JFET and a Low Voltage Si MOSFET into a single TO-247-4L package. This innovative approach allows users to create circuitry that would enable a normally-off switch while leveraging the benefits of a normally-on SiC JFET. These benefits include ultra-low on-resistance ($R_{DS(on)}$) to minimize conduction losses and the exceptional robustness characteristic of a simplified JFET device structure, making it capable of handling the high-energy switching required in circuit protection applications. For switch-mode power conversion application, this device provides separate access to the JFET and MOSFET gates for improved speed control and ease of paralleling multiple devices.

Features

- Low $R_{DS(on)}$
- Normally-off capability
- Improved speed control
- Improved parallel device operation (3+ FETs)
- Operating temperature: 175°C (max)
- High pulse current capability
- Excellent device robustness
- Silver-sintered die attach for excellent thermal resistance
- Short circuit rated
- AECQ Qualified

Typical applications

- Solid State / Semiconductor Circuit Breaker
- Solid State / Semiconductor Relay
- Battery Disconnects
- Surge Protection
- Inrush Current Control
- High power switch mode converters (>25kW)

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		750	V
JFET Gate (JG) to source voltage	V_{JGS}	DC	-30 to +3	V
		AC [1]	-30 to +30	V
MOSFET Gate (G) to source voltage	V_{GS}	DC	-20 to +20	V
		AC (f > 1Hz)	-25 to +25	V
Continuous drain current [2]	I_D	T_C = 25°C	104	A
		T_C = 100°C	75	A
Pulsed drain current [3]	I_{DM}	T_C = 25°C	300	A
Single pulsed avalanche energy [4]	E_{AS}	L=15mH, I_{AS} = 4.5A	151	mJ
Power dissipation	P_{tot}	T_C = 25°C	357	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T_J,T_{STG}		-55 to 175	°C
Max. lead temperature for soldering,	T_L		250	°C

1. +30V AC rating applies for turn-on pulses <200ns applied with external R_G > 1Ω.
2. Limited by $T_{J,max}$
3. Pulse width t_p limited by $T_{J,max}$
4. Starting T_J = 25°C

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.33	0.42	°C/W

Electrical Characteristics (T_J = +25°C and V_{JGS} = 0V unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value Min	Value Typ	Value Max	Units
Drain-source breakdown voltage	BV_{DS}	V_{GS}=0V, V_{JGS}=0V, I_D=1mA	750			V
Total drain leakage current	I_{DSS}	V_{DS}=750V, V_{GS}=0V, V_{JGS}=0V, T_J=25°C		3.5	60	μA
		V_{DS}=750V, V_{GS}=0V, V_{JGS}=0V, T_J=175°C		45		
Total JFET gate leakage current	I_{JGSS}	V_{JGS}=-20V, V_{GS}=+12V		0.1	55	μA
Total MOSFET gate leakage current	I_{GSS}	V_{GS}=-20V / +20V		2	20	μA
Drain-source on-resistance	$R_{DS(on)}$	V_{GS}=12V, I_D=60A, V_{JGS}=2V, T_J=25°C		10		mΩ
		V_{GS}=12V, I_D=60A, T_J=25°C		11	14.2	
		V_{GS}=12V, I_D=60A, T_J=125°C		18.4		
		V_{GS}=12V, I_D=60A, T_J=175°C		24.2		
JFET gate threshold voltage	$V_{JG(th)}$	V_{DS}=5V, V_{GS}=12V, I_D=85mA	-11.3	-9.3	-6.7	V
MOSFET gate threshold voltage	$V_{G(th)}$	V_{DS}=5V, V_{JGS}=0V, I_D=10mA	3.5	4.5	5.5	V
JFET gate resistance	R_{JG}	f=1MHz, open drain		0.7		Ω
MOSFET gate resistance	R_G	f=1MHz, open drain		2.3		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value Min	Value Typ	Value Max	Units
Diode continuous forward current [1]	I_S	T_C = 25°C			104	A
Diode pulse current [2]	$I_{S,pulse}$	T_C = 25°C			300	A
Forward voltage	V_{FSD}	V_{GS}=0V, V_{JGS}=0V, I_S=30A, T_J=25°C		1.1	1.24	V
		V_{GS}=0V, V_{JGS}=0V, I_S=30A, T_J=175°C		1.2		
Reverse recovery charge	Q_{rr}	V_{DS}=400V, I_S=60A, V_{GS}=0V, V_{JGS}=0V, R_{JG}=0.7Ω, di/dt=2800A/μs, T_J=25°C		242		nC
Reverse recovery time	t_{rr}			58		ns
Reverse recovery charge	Q_{rr}	V_{DS}=400V, I_S=60A, V_{GS}=0V, V_{JGS}=0V, R_{JG}=0.7Ω, di/dt=2800A/μs, T_J=150°C		280		nC
Reverse recovery time	t_{rr}			89		ns

Typical Performance - Dynamic with MOSFET gate as control terminal and V_{JGS}=0V

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
MOSFET input capacitance	C_{iss}	V_{DS}=400V, V_{GS}=0V, V_{JGS}=0V, f=100kHz		3245		pF
Output capacitance	C_{oss}			178		
Reverse transfer capacitance	C_{rss}			1.2		
Effective output capacitance, energy	$C_{oss(er)}$	V_{DS}=0V to 400V, V_{GS}=0V, V_{JGS}=0V		225		pF
Effective output capacitance, time related	$C_{oss(tr)}$			470		pF
C_{OSS} stored energy	E_{oss}	V_{DS}=400V, V_{GS}=0V, V_{JGS}=0V		18		μJ
Total Gate charge	Q_G	V_{DS}=400V, I_D=60A, V_{JGS}=0V, V_{GS} = 0V to 15V		75		nC
Gate-drain charge	Q_{GD}			13		
Gate-source charge	Q_{GS}			22		
Turn-on delay time	$t_{d(on)}$	Notes 5 and 6 V_{DS}=400V, I_D=60A, V_{GS}=0V to +15V, R_{G_ON}=1Ω, R_{G_OFF}=10Ω, R_{JG_ON}=0.7Ω, R_{JG_OFF}=4.7Ω, Inductive Load, FWD: same device with V_{GS} = 0V, R_G =10Ω, V_{JGS}=0V, R_{JG}=0.7Ω, T_J=25°C		50		ns
Rise time	t_r			21		
Turn-off delay time	$t_{d(off)}$			107		
Fall time	t_f			33		
Turn-on energy	E_{ON}			990		μJ
Turn-off energy	E_{OFF}			513		
Total switching energy	E_{TOTAL}			1503		
Turn-on delay time	$t_{d(on)}$	Notes 5 and 6 V_{DS}=400V, I_D=60A, V_{GS}=0V to +15V, R_{G_ON}=1Ω, R_{G_OFF}=10Ω, R_{JG_ON}=0.7Ω, R_{JG_OFF}=4.7Ω, Inductive Load, FWD: same device with V_{GS} = 0V, R_G =10Ω, V_{JGS}=0V, R_{JG}=0.7Ω, T_J=150°C		50		ns
Rise time	t_r			22		
Turn-off delay time	$t_{d(off)}$			110		
Fall time	t_f			30		
Turn-on energy	E_{ON}			986		μJ
Turn-off energy	E_{OFF}			454		
Total switching energy	E_{TOTAL}			1440		

5. Measured with the half-bridge mode switching test circuit in Figure 23.
6. Devices are driven with the ClampDRIVE method as descriped in the section "Recommended Gate Drive Approach: ClampDRIVE method".

Typical Performance - Dynamic with JFET gate as control terminal and V_{GS}=+12V

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
JFET input capacitance	C_{Jiss}	V_{DS}=400V, V_{JGS}=-20V, f=100kHz		1385		pF
JFET output capacitance	C_{Joss}			175		
JFET reverse transfer capacitance	C_{Jrss}			170		
JFET total gate charge	Q_{JG}	V_{DS}=400V, I_D=60A, V_{JGS} = -18V to 0V		223		nC
JFET gate-drain charge	Q_{JGD}			126		
JFET gate-source charge	Q_{JGS}			35		

Typical Performance Diagrams - MOSFET gate as control terminal and V_{JGS}=0V

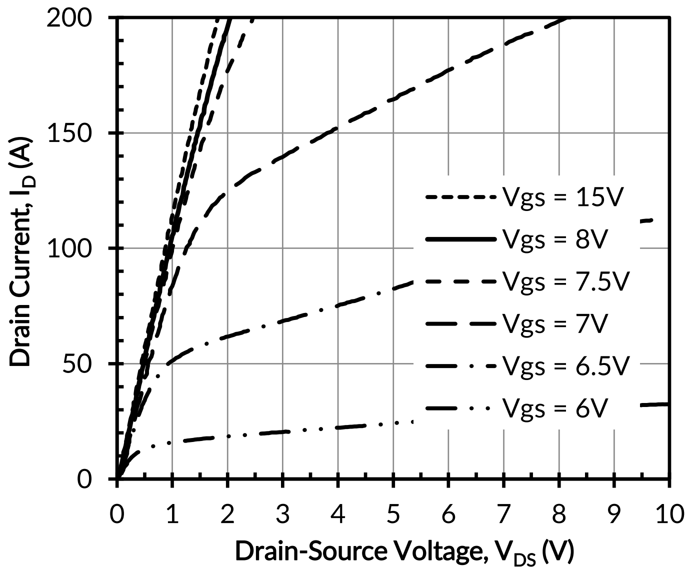


Figure 1. Typical output characteristics at T_J = - 55°C, tp < 250µs

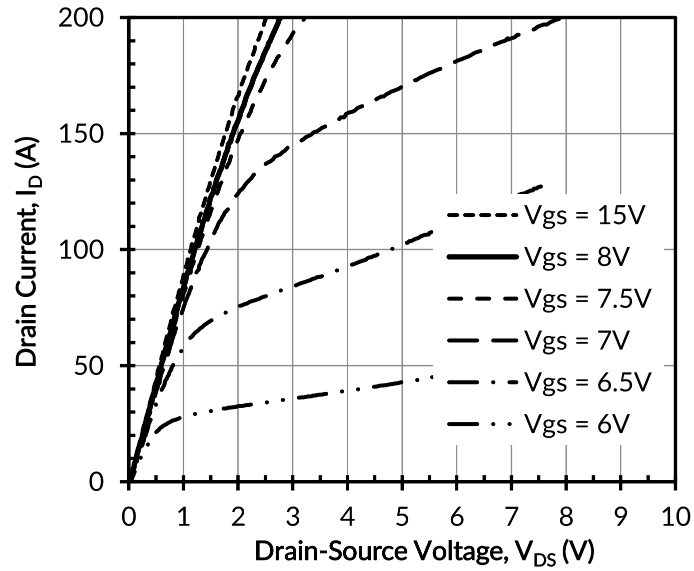


Figure 2. Typical output characteristics at T_J = 25°C, tp < 250µs

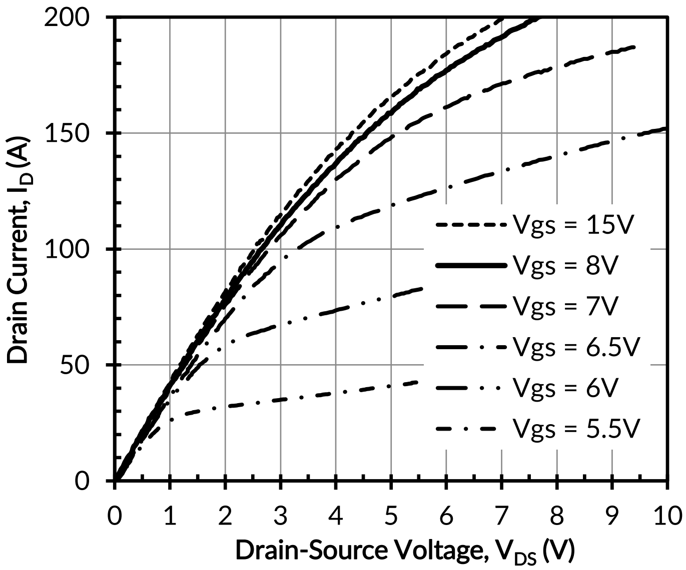


Figure 3. Typical output characteristics at T_J = 175°C, tp < 250µs

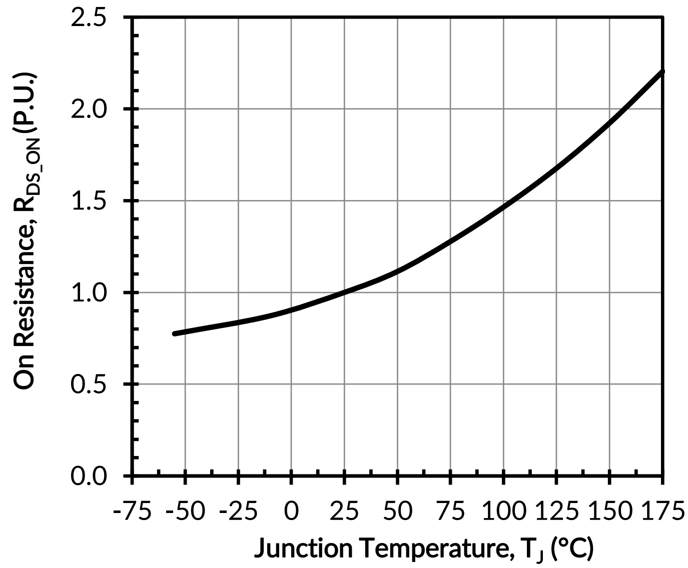


Figure 4. Normalized on-resistance vs. temperature at V_{GS} = 12V and I_D = 60A

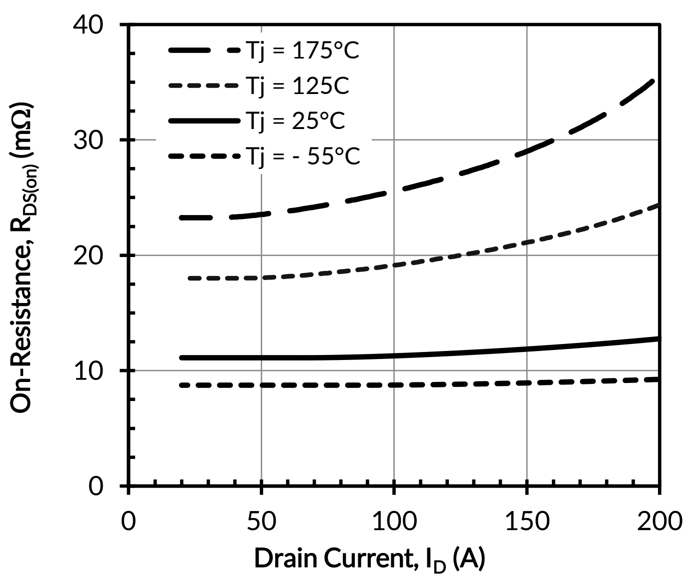


Figure 5. Typical drain-source on-resistances at V_{GS} = 12V

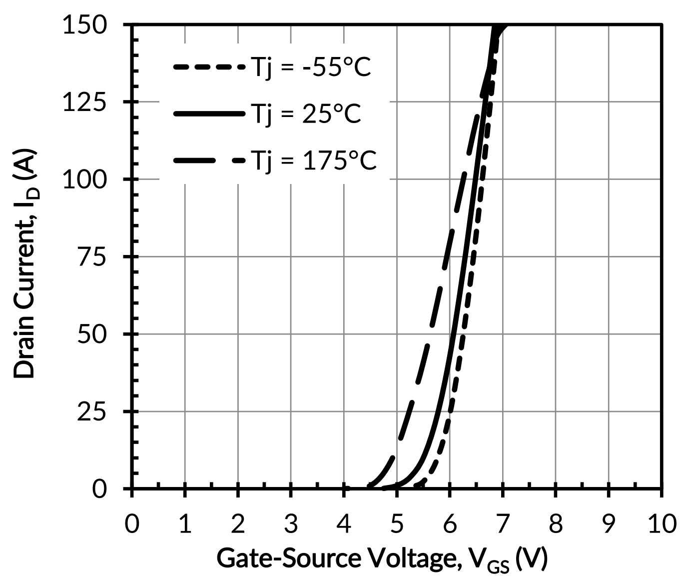


Figure 6. Typical transfer characteristics at V_{DS} = 5V

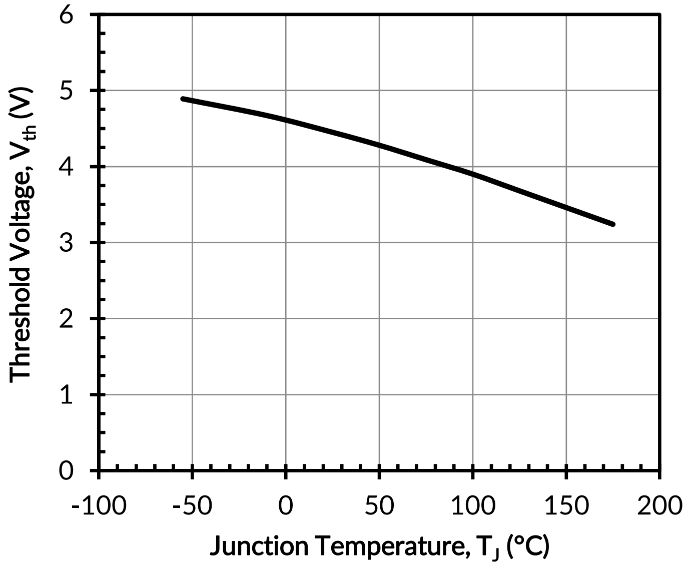


Figure 7. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_D = 10mA

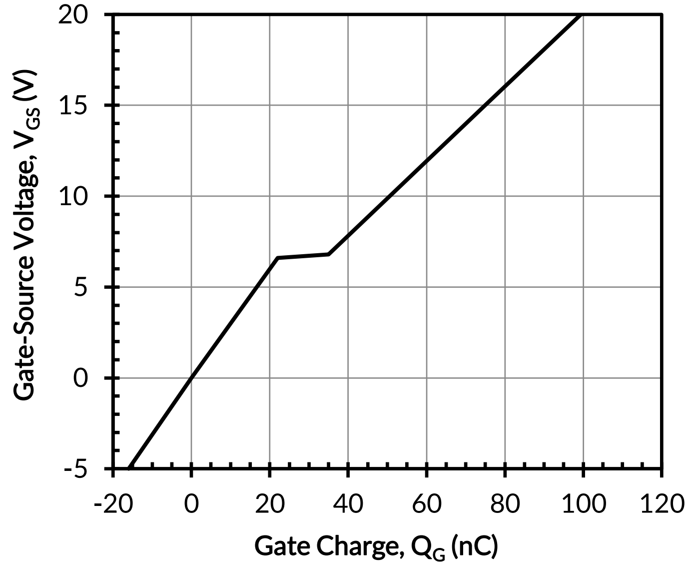


Figure 8. Typical gate charge at V_{DS}=400V and I_D = 60A

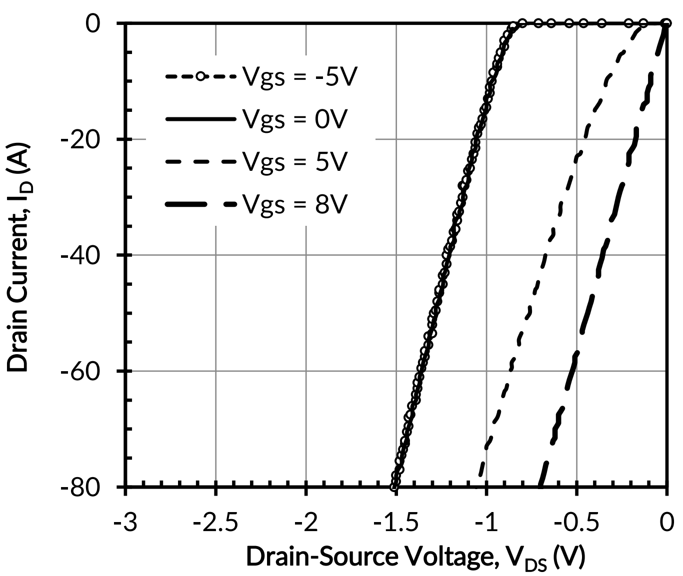


Figure 9. 3rd quadrant characteristics at T_J = -55°C

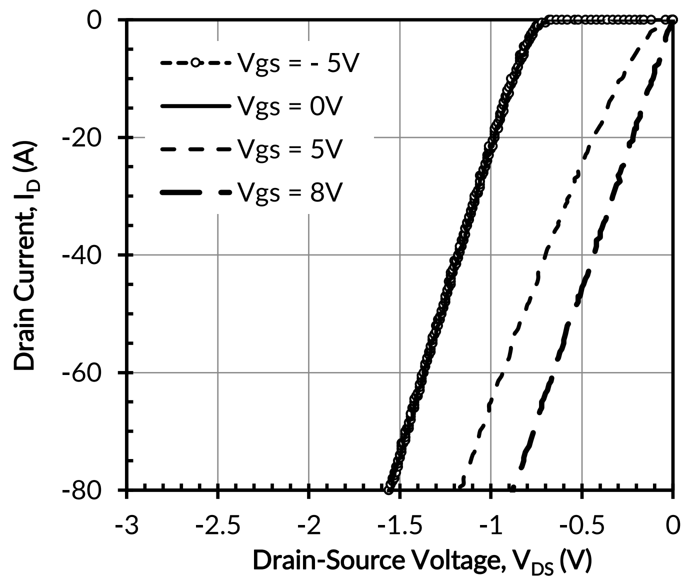


Figure 10. 3rd quadrant characteristics at T_J = 25°C

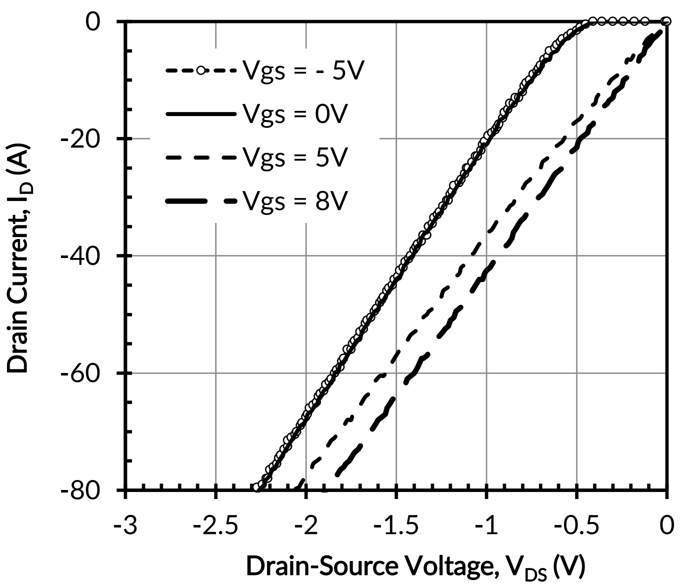


Figure 11. 3rd quadrant characteristics at T_J = 175°C

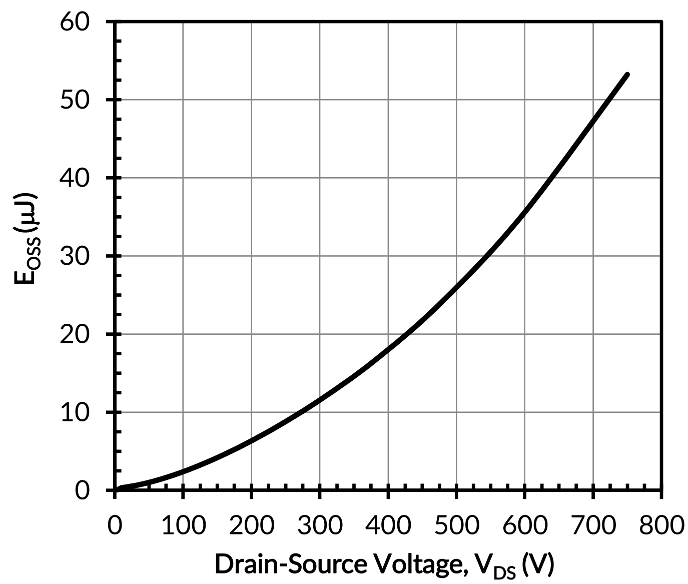


Figure 12. Typical stored energy in C_{OSS} at V_{GS} = 0V

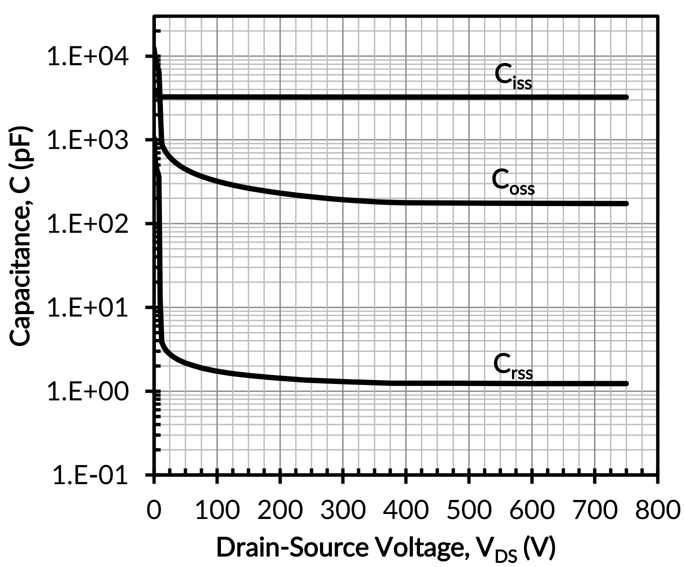


Figure 13. Typical capacitances at f = 100kHz and V_{GS} = 0V

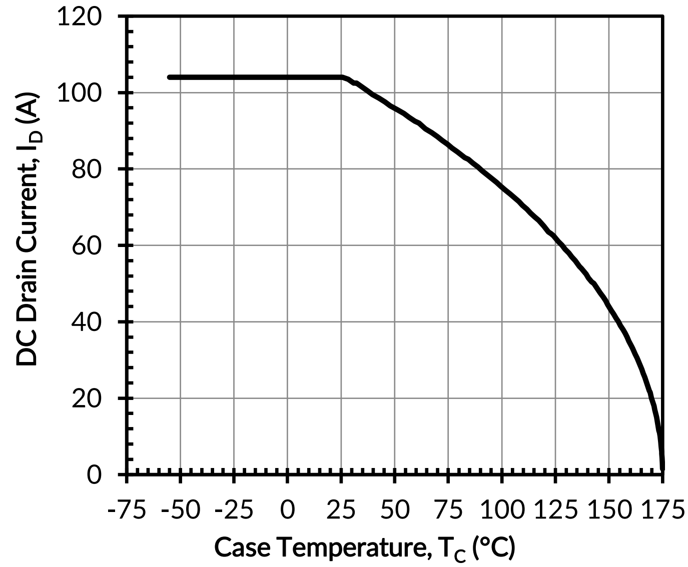


Figure 14. DC drain current derating

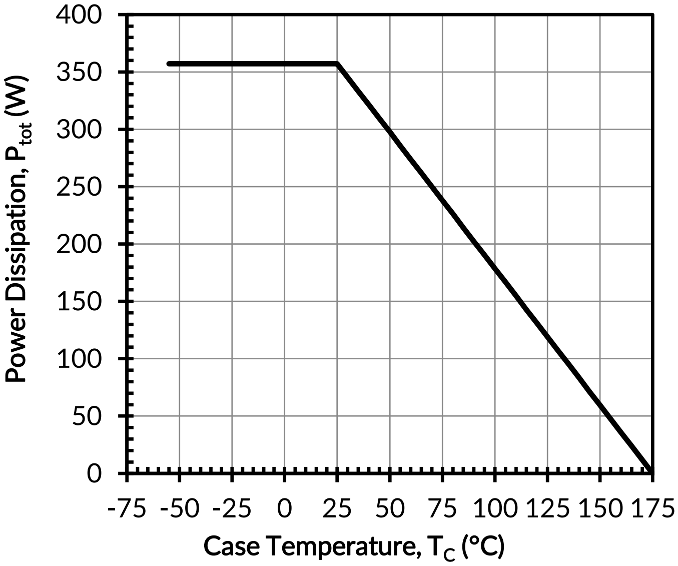
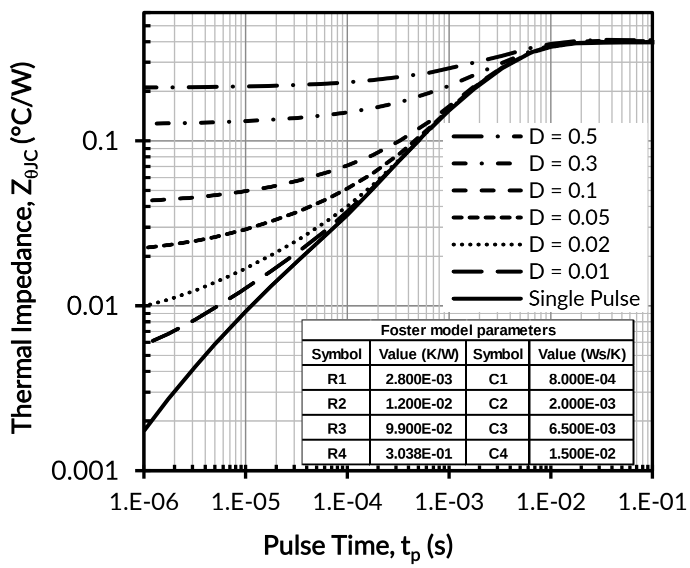


Figure 15. Total power dissipation



Foster model parameters

Symbol	Value (K/W)	Symbol	Value (Ws/K)
R1	2.800E-03	C1	8.000E-04
R2	1.200E-02	C2	2.000E-03
R3	9.900E-02	C3	6.500E-03
R4	3.038E-01	C4	1.500E-02

Figure 16. Maximum transient thermal impedance

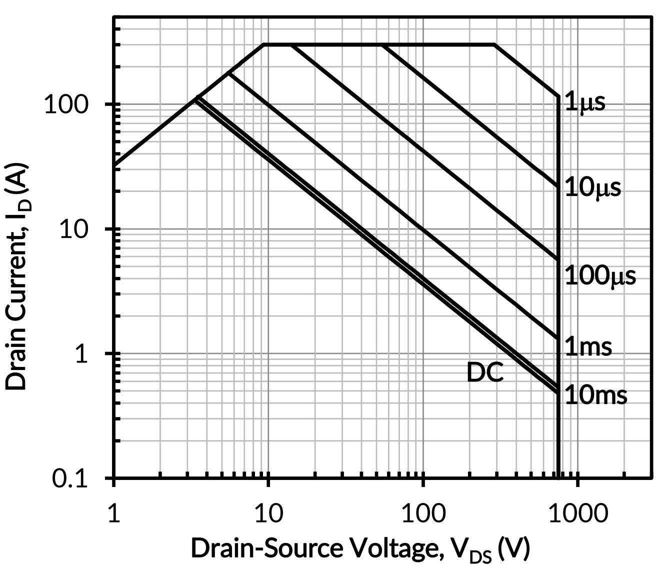


Figure 17. Safe operation area at T_C = 25°C, D = 0, Parameter t_p

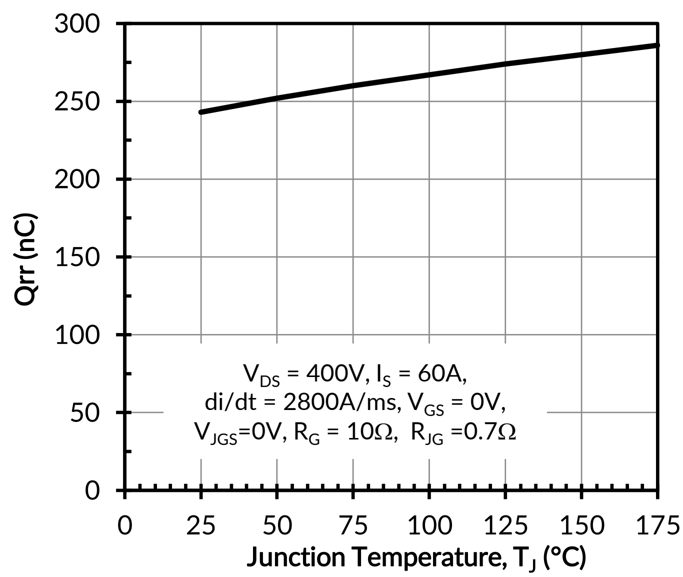


Figure 18. Reverse recovery charge Qrr vs. junction temperature

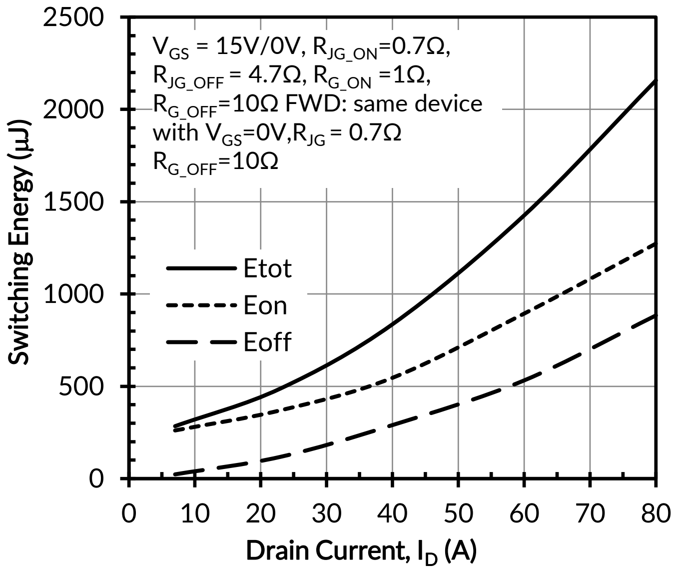


Figure 19. Clamped inductive switching energy vs. drain current at V_{DS} = 400V and T_J = 25°C

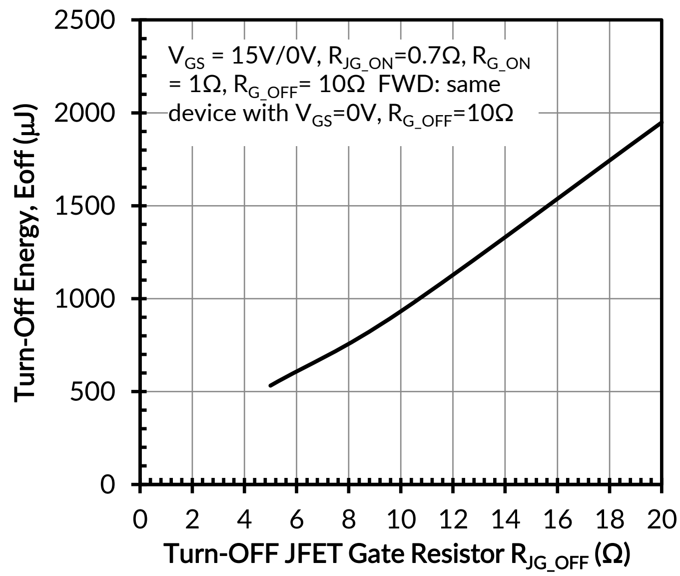


Figure 20. Clamped inductive switching turn-off energy vs. JFET gate resistor R_{JG_OFF} at V_{DS} = 400V, I_D = 60A, and T_J = 25°C

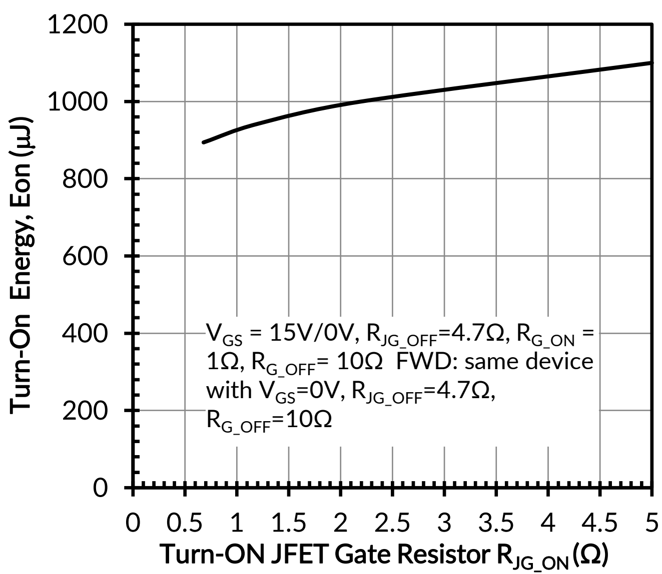


Figure 21. Clamped inductive switching turn-on energy vs. JFET gate resistor R_{JG_ON} at V_{DS} = 400V, I_D = 60A, and T_J = 25°C

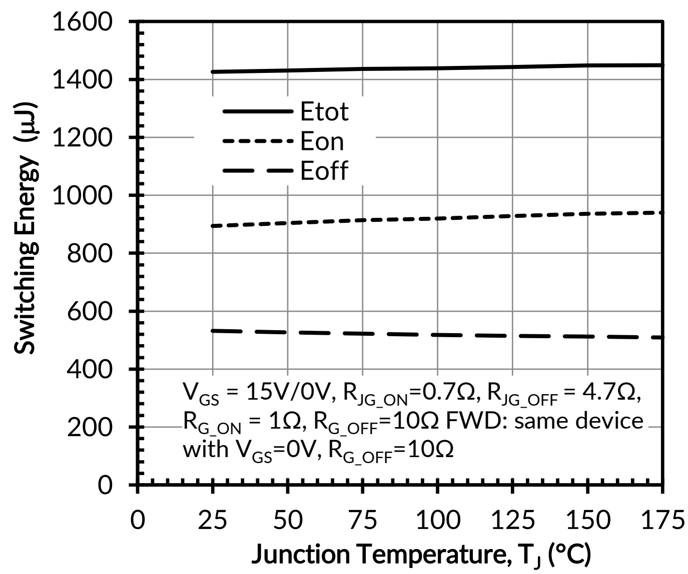


Figure 22. Clamped inductive switching energy vs. junction temperature at V_{DS} = 400V and I_D = 60A

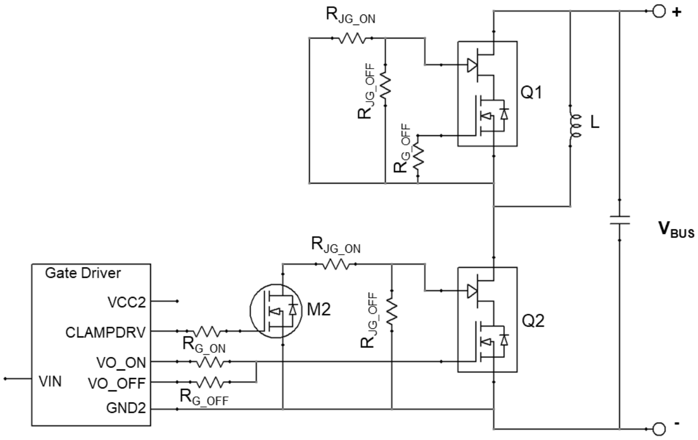


Figure 23. Schematic of the half-bridge mode switching test circuit with ClampDRIVE method.

Typical Performance Diagrams - JFET gate as control terminal and V_{GS}=+12V

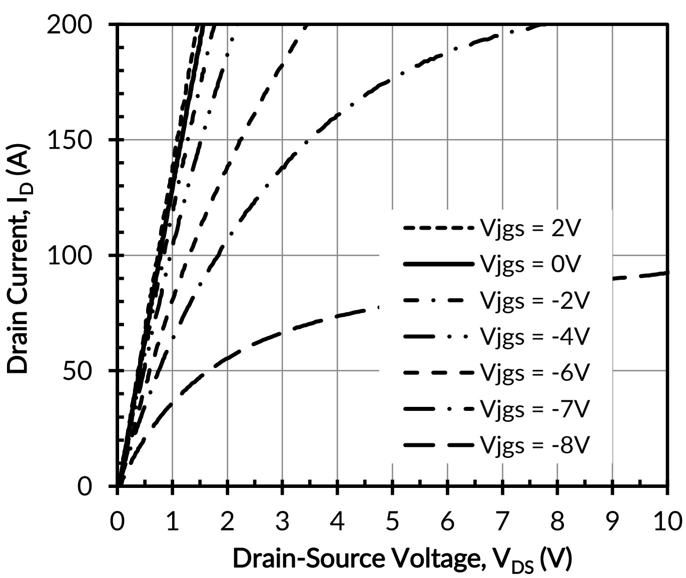


Figure 24. Typical output characteristics with JFET

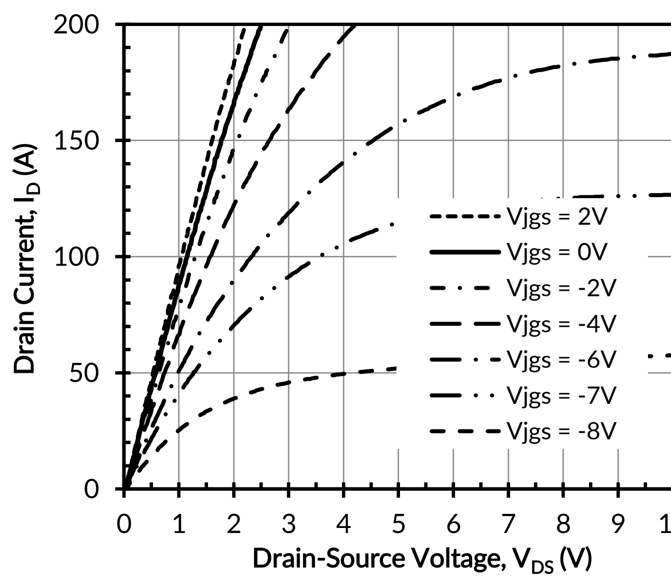


Figure 25. Typical output characteristics with JFET

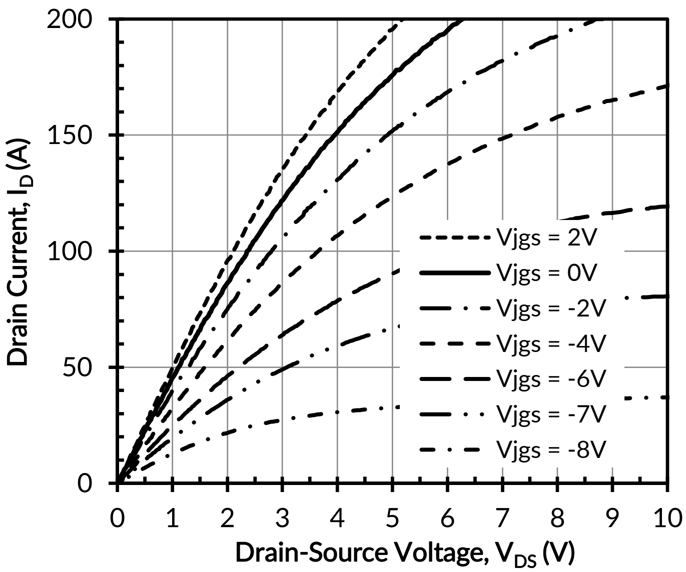


Figure 26. Typical output characteristics with JFET gate as control at T_J = 175°C, t_p < 250µs

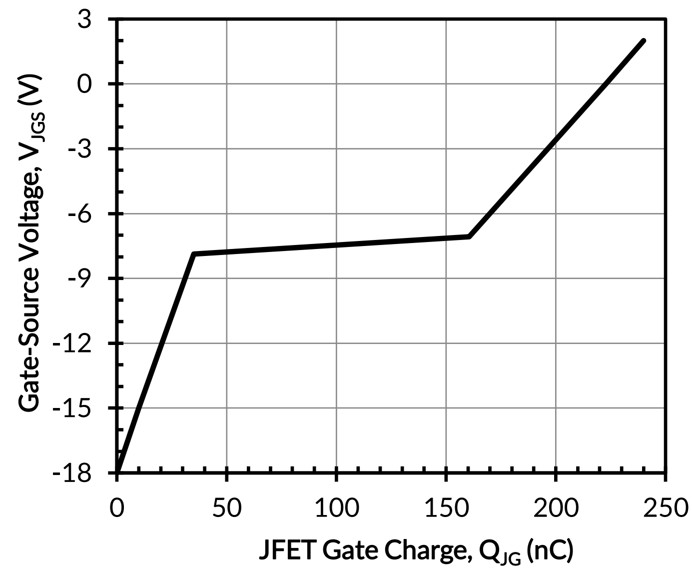


Figure 27. Typical JFET gate charge at V_{DS} = 400V and I_D = 60A

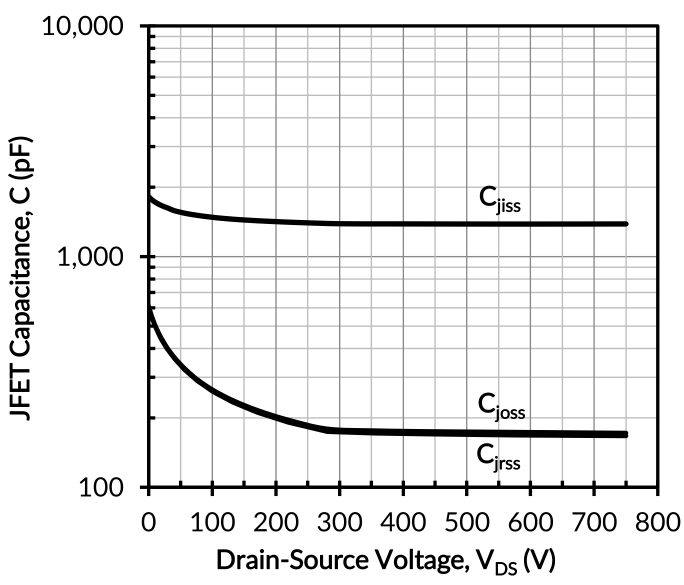


Figure 28. Typical JFET capacitances at f = 100kHz and V_{JGS} = -20V

Recommended Gate Drive Approach: ClampDRIVE method

Since both JFET gate and MOSFET gate are accessible, more parameters and approaches can be used to control the switching behaviors of the device and make the device suitable for a wide range applications from solid state circuit breakers requiring ultra-high current turn-off capability to motor drives requiring fast switching speed. The recommended gate drive approach is the ClampDRIVE method, with which the desired turn-on speed, turn-off speed and reverse recovery performance can be achieved at the same time. The main idea of this method is to dynamically tune the JFET gate resistor value R_{JG} such that, in the off-state, R_{JG} is small enough not to cause a reverse recovery issue, and during turn-off transient, R_{JG} is set to a higher value for the desired turn-off performance. This method can be easily implemented using a commercial off-the-shelf gate driver with miller clamp pre-driver output, as illustrated in Figure A. VIN is the gate driver input signal. VO is the gate driver output and CLAMPDRV is the gate driver miller clamp pre-driver output. M2 is the clamp MOSFET used to control the JFET gate resistance. The MOSFET M2 is directly controlled by the CLAMPDRV signal.

In the on-state, CLAMPDRV is low which turns the MOSFET M2 off, thus, the effective JFET gate resistance is R_{JG_OFF}. During the turn-off transient, CLAMPDRV is kept low until the device is fully off. This means the JFET gate resistance is R_{JG_OFF} during the turn-off process, and R_{GJ_OFF} can be used to effectively control turn-off speed. After the device is fully off, CLAMPDRV is changed to high level, which turns the MOSFET M2 on.

In the off-state, CLAMPDRV is high and the clamp MOSFET M2 is in on-state. The effective JFET gate resistance is equal to the parallel combination of R_{JG_OFF} and R_{JG_ON}. R_{JG_ON} can be selected small enough to prevent the reverse recovery issue. During the turn-on transient, the JFET gate current may flow from the cascode source through the body diode of the MOSFET M2 and R_{JG_ON} into the JFET gate, so, the turn-on process is also determined by R_{JG_ON}.

In summary, the optimum switching performance of the SiC cascode FETs can be realized with the ClampDRIVE method by selecting proper JFET gate resistors R_{JG_ON} and R_{JG_OFF}.

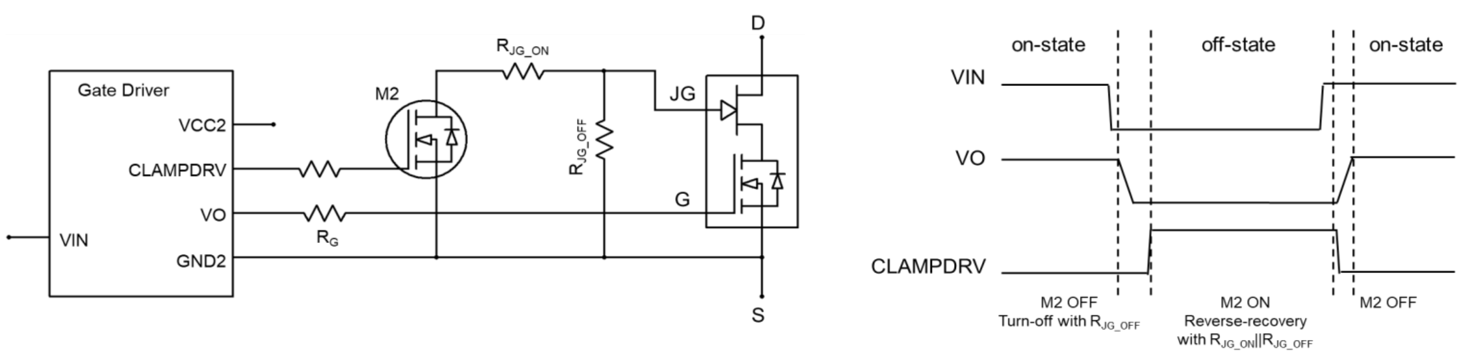
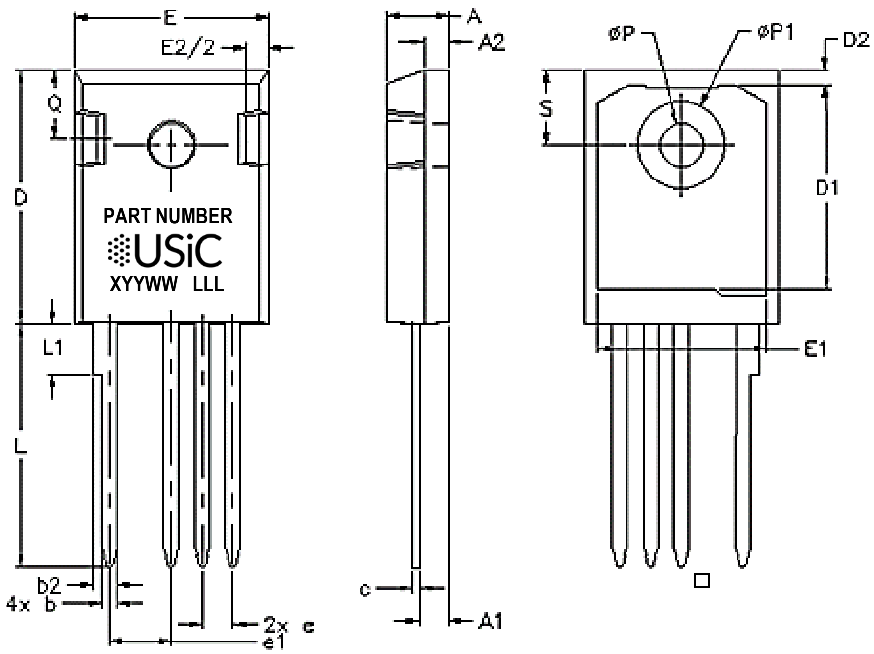


Figure A. Circuit schematic and timing diagram of the ClampDRIVE method

Important notice

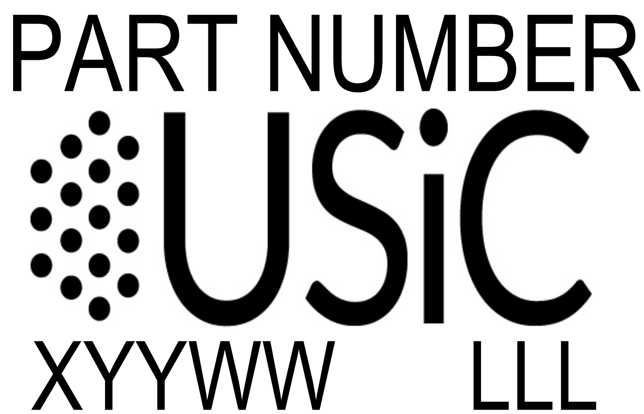
TO-247-4L PACKAGE OUTLINE, PART MARKING AND TUBE SPECIFICATIONS

PACKAGE OUTLINE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.185	0.209	4.7	5.31
A1	0.087	0.102	2.21	2.59
A2	0.059	0.098	1.5	2.49
b	0.039	0.055	0.99	1.4
b2	0.065	0.094	1.65	2.39
c	0.015	0.035	0.38	0.89
D	0.819	0.845	20.8	21.46
D1	0.515	-	13.08	-
D2	0.02	0.053	0.51	1.35
E	0.61	0.64	15.49	16.26
e	0.100 BSC		2.54 BSC	
e1	0.19	0.21	4.83	5.33
E1	0.53	-	13.46	-
E2	0.14	0.16	3.56	4.06
L	0.78	0.8	19.81	20.32
L1	-	0.177	-	4.5
ΦP	0.14	0.144	3.56	3.66
ΦP1	0.278	0.291	7.06	7.39
Q	0.212	0.244	5.38	6.2
S	0.243 BSC		6.17 BSC	

PART MARKING



PART NUMBER = REFER TO DS_PN DECODER FOR DETAILS

X = ASSEMBLY SITE
YY = YEAR
WW = WORK WEEK
LLL = LOT ID

PACKING TYPE

ANTI-STATIC TUBE

QUANTITY /TUBE : 30 UNITS

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