

SiC JFET Division

Is Now Part of



To learn more about onsemi™, please visit our website at www.onsemi.com

onsemi and ONSEMI. and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries. onsemi owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of onsemi product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. onsemi reserves the right to make changes at any time to any products or information herein is provided "as-is" and onsemi makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using onsemi products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by onsemi. "Typical" parameters which may be provided in onsemi data sheets and/ or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. onsemi does not convey any license under any of its intellectual property rights nor the rights of others. onsemi products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use onsemi products for any such unintended or unauthorized application,















Silicon Carbide (SiC) Cascode JFET Module - EliteSiC, Half-Bridge Module, 1200 V, 19 mohm

Rev. D, January 2025

Description

This SiC FET device is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's silicon-like gate-drive characteristics allows the use of unipolar gate drives, compatible with Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the E1B module package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads, and any application requiring standard gate drive. Advanced Ag sintering die attach technology gives the module superior thermal performance.

Features

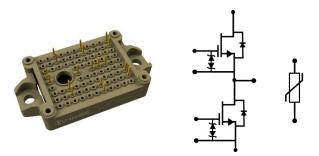
- On-resistance: $R_{DS(on)} = 19m\Omega$ (typ)
- Operating temperature: 150°C (max)
- Excellent reverse recovery: Q_{rr} = 495nC
- Low body diode voltage: V_{FSD}= 1.2V
- Low gate charge: Q_G = 85nC
- Threshold voltage V_{G(th)}: 5V (typ) allowing 0 to 15V drive
- Low intrinsic capacitance
- ESD protected: HBM class 2 and CDM class C3
- AECQ Qualified

Typical applications

- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating



UHB50SC12E1BC3N



Part Number	Package	Marking
UHB50SC12E1BC3N	E1B	UHB50SC12E1BC3N



















Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		1200	V
Gate-source voltage	V	DC	-20 to +20	V
Gate-source voltage	V_{GS}	AC (f > 1Hz)	-25 to +25	V
Continuous drain current ¹	l _D	T _C = 25°C	69	Α
		T _C = 85°C	50	Α
Pulsed drain current ²	I _{DM}	T _C = 25°C	350	Α
Power dissipation per switch	P _{tot}	T _C = 25°C	208	W
Maximum junction temperature	$T_{J,max}$		150	°C
Operating and storage temperature	T _J , T _{STG}		-55 to 150	°C

- 1. Limited by $T_{J,max}$
- 2. Pulse width t_p limited by $T_{J,max}$

Thermal Characteristics

Parameter	Symbol	Test Conditions		Units		
			Min	Тур	Max	Units
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.46	0.6	°C/W

NTC Thermistor Characteristics

Parameter	Symbol	Test Conditions		Units		
			Min	Тур	Max	Units
Rated resistance	R ₂₅	T _{NTC} = 25°C		5		kΩ
Resistance value tolerance	ΔR/R	T _{NTC} = 25°C	-5		5	%
Power dissipation	P ₂₅	T _{NTC} = 25°C			20	mW
B constant	B _{25/50}	$R_2 = R_{25} \exp [B_{25/50} (1/T_2 - 1/(298.15 K))]$		3375		К

Module

Parameter	Symbol	Test Conditions	Value	Units
Isolation voltage	V _{ISOL}	RMS, f = 50 Hz, t = 1 min	3	kV
Internal isolation			Al ₂ O ₃	
Creepage distance		Terminal to heatsink	12.7	na na
		Terminal to terminal	6.3	mm
Clearance distance		Terminal to heatsink	10	mm
Clearance distance		Terminal to terminal	5	mm
Stray inductance module	L _{sCE}		11	nΗ













SiC FET Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions		Value		
Parameter	Symbol	rest Conditions	Min	Тур	Max	Units
Drain-source breakdown voltage	BV _{DS}	V_{GS} =0V, I_D =4mA	1200			V
		V _{DS} =1200V,		17	000	
Total drain leakage current		V _{GS} =0V, T _J =25°C		16	300	μА
Total dialif leakage culterit	I _{DSS}	V _{DS} =1200V,		50		μΑ
		V _{GS} =0V, T _J =150°C		30		
Total gate leakage current	I _{GSS}	V _{DS} =0V, T _J =25°C,		12	40	^
Total gate leakage current		V _{GS} =-20V / +20V				μА
		V _{GS} =12V, I _D =50A,		19	24	
		T _J =25°C				
Drain course on recistance	D	V_{GS} =12V, I_{D} =50A,		30	0	mΩ
Drain-source on-resistance	R _{DS(on)}	T _J =125°C		30		
		$V_{GS}=12V, I_{D}=50A,$		35		
		T _J =150°C		ა <u>ა</u>		
Gate threshold voltage	V _{G(th)}	V_{DS} =5V, I_D =20mA	4	5	6	V
Gate resistance	R_G	f=1MHz, open drain		2.2		Ω

Typical Performance - Reverse Diode

Parameter	Symbol			Units		
Parameter	Symbol		Units			
Diode continuous forward current ¹	I _S	T _C = 25°C			69	Α
Diode pulse current ²	$I_{S,pulse}$	T _C = 25°C			350	Α
		V_{GS} =0V, I_{S} =25A,		1.2	1 /	
Forward voltage	V	$V_{FSD} = \begin{array}{c c} T_J = 25^{\circ}C & & & & \\ \hline V_{GS} = 0V, \ I_S = 25A, & & & 1.4 \end{array}$	1.4	V		
Forward voitage	V FSD	V _{GS} =0V, I _S =25A,		1.4		V
		T _J =150°C				
Reverse recovery charge	Q _{rr}	V _R =800V, I _S =50A,		105		nC
Reverse recovery charge		V_{GS} =-5V, R_{G_EXT} =20 Ω ,		473		IIC
Reverse recovery time	t _{rr}	di/dt=4000A/μs,		21		nc
Reverse recovery time		T _J =25°C	21			ns
Poverce recovery charge		V _R =800V, I _S =50A,		145		20
Reverse recovery charge	Q_{rr}	V_{GS} =0V, R_{G_EXT} =20 Ω ,	465	403		nC
Davonas na savom timas	1	di/dt=4000A/μs,		22		
Reverse recovery time	t _{rr}	T _J =150°C		22		ns













Typical Performance - Dynamic

D	6 1 1	T I C I''	Value			11-24-
Parameter	Symbol	Test Conditions –	Min	Тур	Max	Units
Input capacitance	C_{iss}	\/ 000\/ \/ 0\/		2930		
Output capacitance	C_{oss}	V _{DS} =800V, V _{GS} =0V f=100kHz		187		pF
Reverse transfer capacitance	C _{rss}	1 1001(1)2		3.3		
Effective output capacitance, energy related	C _{oss(er)}	V _{DS} =0V to 800V, V _{GS} =0V		240		pF
Effective output capacitance, time related	$C_{oss(tr)}$	V _{DS} =0V to 800V, V _{GS} =0V		533		pF
C _{OSS} stored energy	E _{oss}	V _{DS} =800V, V _{GS} =0V		77		μJ
Total gate charge	Q_{G}	V _{DS} =800V, I _D =50A, V _{GS} = -5V to 15V		85		
Gate-drain charge	Q_{GD}			19		nC
Gate-source charge	Q_{GS}			31		
Turn-on delay time	t _{d(on)}	Notes 3 and 4 V _{DS} =800V, I _D =50A, Gate Driver =-5V to +15V,		22		
Rise time	t _r			18		ns
Turn-off delay time	t _{d(off)}			65		
Fall time	t _f	R_{G_EXT} =10 Ω , inductive Load,		10		
Turn-on energy	E _{ON}	FWD: same device with		843		
Turn-off energy	E _{OFF}	$V_{GS} = 0V$ and $R_{G_EXT} = 10\Omega$,		139		- μJ
Total switching energy	E _{TOTAL}	T _J =25°C		982		
Turn-on delay time	t _{d(on)}	Notes 3 and 4		22		
Rise time	t _r	V _{DS} =800V, I _D =50A, Gate		16		
Turn-off delay time	t _{d(off)}	Driver =-5V to +15V, $R_{G_{EXT}}=10\Omega,$ inductive Load,		67		ns
Fall time	t _f			12		
Turn-on energy	E _{ON}	FWD: same device with		805		
Turn-off energy	E _{OFF}	V_{GS} = 0V and R_{G_EXT} =10 Ω ,		125		μJ
Total switching energy	E _{TOTAL}	T _J =150°C		930		

^{3.} Measured with the half-bridge mode switching test circuit in Figure 23.

^{4.} A bus RC snubber (R_{BS} = 2.5 Ω , C_{BS} =200nF) must be applied to reduce the power loop high frequency oscillations.













Typical Performance - Dynamic (continued)

Parameter	Symbol	Test Conditions	Value			Units
	Зуппоп	rest Conditions	Min	Тур	Max	Offics
Turn-on delay time	t _{d(on)}	Notes 5 and 6,		32		
Rise time	t _r	V _{DS} =800V, I _D =50A, Gate		24		nc
Turn-off delay time	t _{d(off)}	Driver =-5V to +15V,		40		ns
Fall time	t _f	Turn-on $R_{G,EXT} = 2\Omega$,		20		
Turn-on energy including R _S energy	E _{ON}	Turn-off $R_{G,EXT}$ =2 Ω , inductive Load,		738		
Turn-off energy including R_{S} energy	E _{OFF}	FWD: same device with		260		
Total switching energy	E _{TOTAL}	$V_{GS} = 0V$ and $R_G = 2\Omega$, RC		998		μЈ
Snubber R _S energy during turn-on	E _{RS_ON}	snubber: R_s =5 Ω and C_s =150pF, T_J =25°C		10		
Snubber R _S energy during turn-off	E _{RS_OFF}			5		
Turn-on delay time	t _{d(on)}	Notes 5 and 6,		30		
Rise time	t _r	V _{DS} =800V, I _D =50A, Gate		21		ns
Turn-off delay time	t _{d(off)}	Driver =-5V to +15V,		41		115
Fall time	t _f	Turn-on $R_{G,EXT} = 2\Omega$, Turn-off $R_{G,EXT} = 2\Omega$, inductive Load, FWD: same device with $V_{GS} = 0V$ and $R_{G} = 2\Omega$, RC snubber: $R_{S} = 5\Omega$ and		19		
Turn-on energy including R _S energy	E _{ON}			655		
Turn-off energy including R _S energy	E _{OFF}			263		
Total switching energy	E _{TOTAL}			918		μЈ
Snubber R _S energy during turn-on	E _{RS_ON}	C _S =150pF,		11		
Snubber R _s energy during turn-off	E _{RS_OFF}	T _J =150°C		5.5		

^{5.} Measured with the chopper mode switching test circuit in Figure 24.

^{6.} In this table, the switching energies (turn-on energy, turn-off energy and total energy) presented include the device RC snubber energy losses.













SiC FET Typical Performance Diagrams

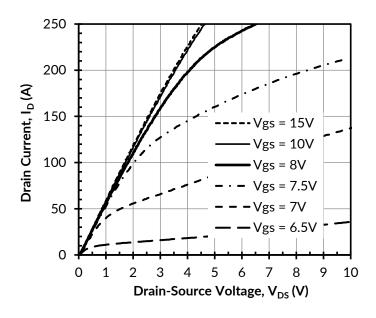


Figure 1. Typical output characteristics at T_J = - 55°C, tp < 250 μ s

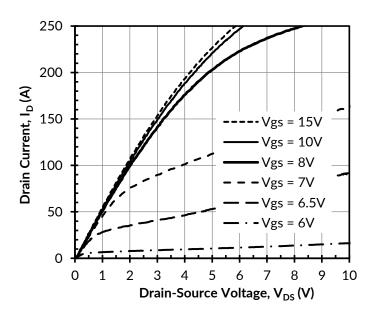


Figure 2. Typical output characteristics at T_J = 25°C, tp < 250 μ s

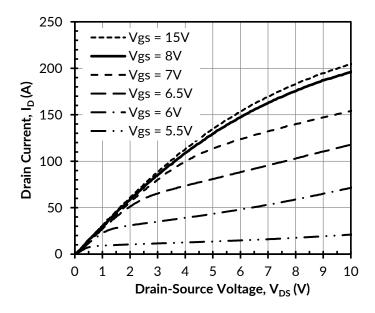


Figure 3. Typical output characteristics at T_J = 150°C, tp < 250 μ s

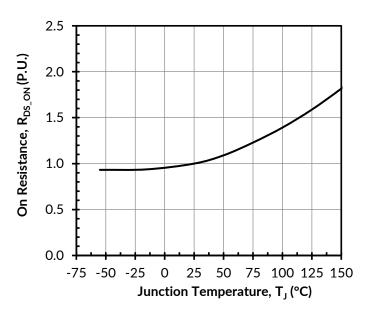


Figure 4. Normalized on-resistance vs. temperature at V_{GS} = 12V and I_D = 50A



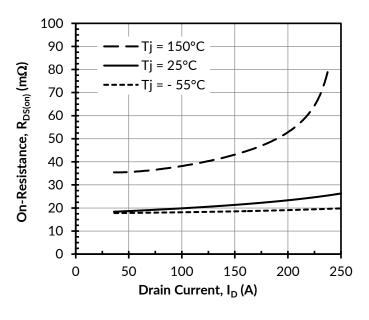








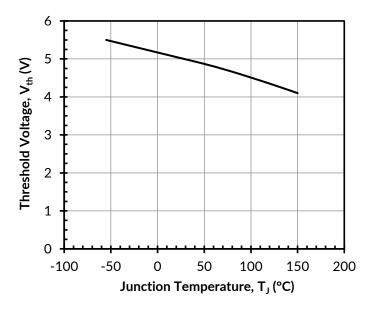




Tj = -55°C Tj = 25°C Drain Current, I_D (A) Tj = 150°C Gate-Source Voltage, V_{GS} (V)

Figure 5. Typical drain-source on-resistances at V_{GS} = 12V

Figure 6. Typical transfer characteristics at $V_{DS} = 5V$



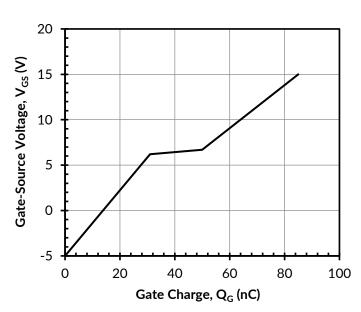


Figure 7. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_{D} = 20mA

Figure 8. Typical gate charge at V_{DS} = 800V and I_{D} = 50A













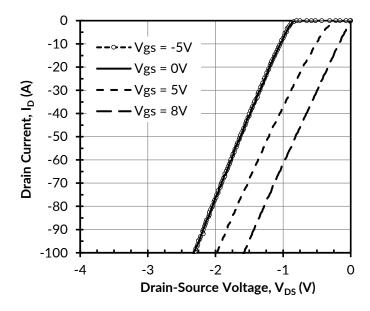


Figure 9. 3rd quadrant characteristics at $T_J = -55$ °C

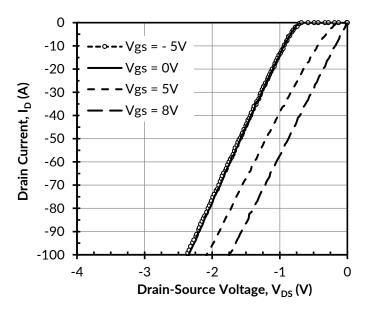


Figure 10. 3rd quadrant characteristics at $T_J = 25$ °C

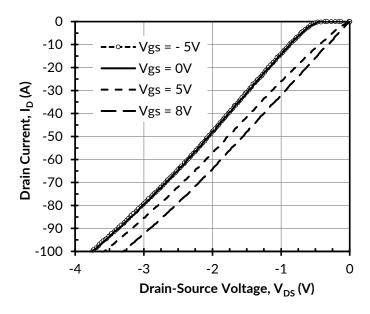


Figure 11. 3rd quadrant characteristics at $T_J = 150$ °C

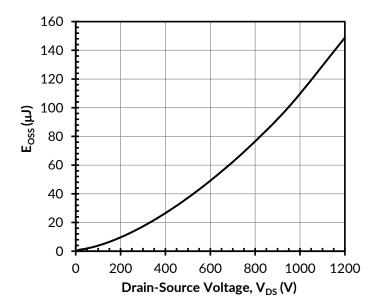


Figure 12. Typical stored energy in C_{OSS} at $V_{GS} = 0V$













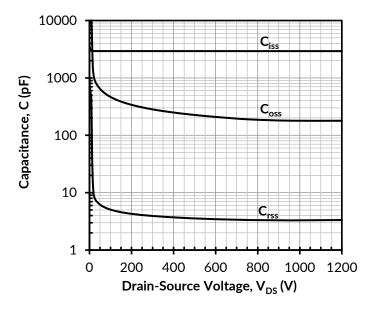


Figure 13. Typical capacitances at f = 100kHz and V_{GS} = 0V

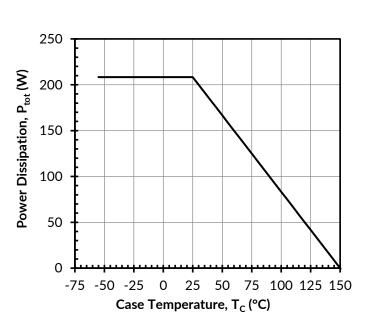


Figure 15. Total power dissipation

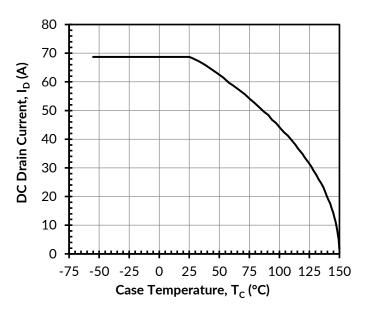


Figure 14. DC drain current derating

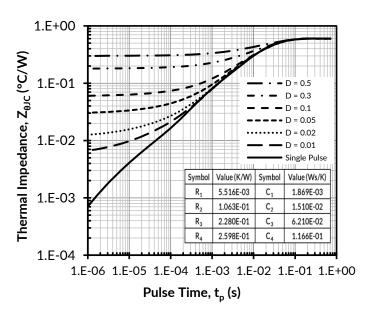


Figure 16. Maximum transient thermal impedance and parameters for thermal equivalent circuit (Foster) model













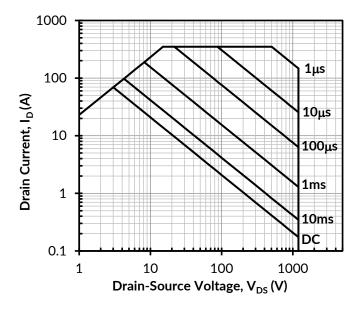


Figure 17. Safe operation area at T_C = 25°C, D = 0, Parameter t_D

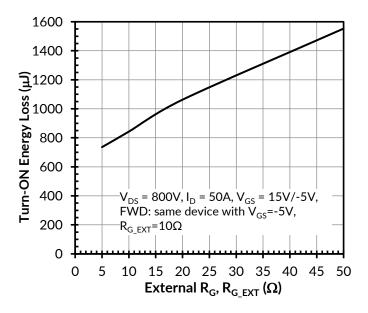


Figure 19. Clamped inductive switching turn-on energy vs. turn-on gate resistance $R_{\rm G}$

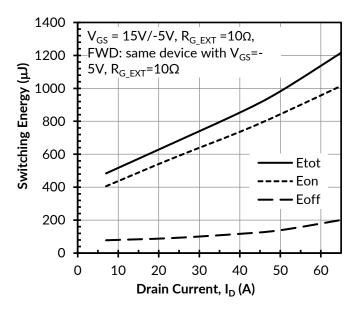


Figure 18. Clamped inductive switching energy vs. drain current at V_{DS} = 800V and T_J = 25°C

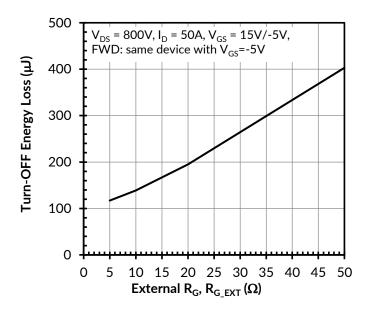


Figure 20. Clamped inductive switching turn-off energy vs. turn-off gate resitiance R_G



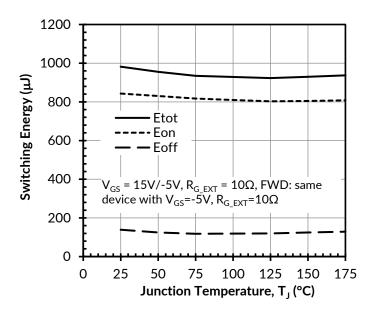








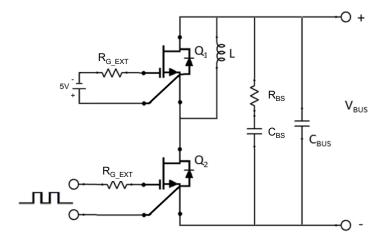




600 500 400 300 $I_{S} = 50A$, di/dt =4000A/μs, 200 $V_{GS}=5V$, $R_{GEXT} = 20\Omega$ 100 0 100 125 150 0 25 50 Junction Temperature, T₁ (°C)

Figure 21. Clamped inductive switching energy vs. junction temperature at V_{DS} = 800V and I_{D} = 50A

Figure 22. Reverse recovery charge Q_{rr} vs. junction temperature at V_{DS} = 800V



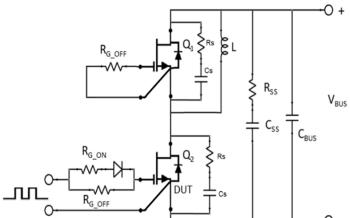


Figure 23. Schematic of the half-bridge mode switching test circuit. Note, a bus RC snubber (R_{BS} = 2.5Ω , C_{BS} =100nF) must be applied to reduce the power loop high frequency oscillations.

Figure 24. Schematic of the half-bridge mode switching test circuit with device RC snubbers (R_s = 5 Ω , C_s = 150pF) and a bus RC snubber (R_{SS} = 2.5 Ω , C_{SS} =100nF).





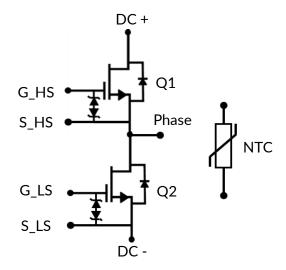


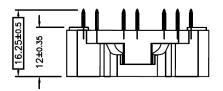




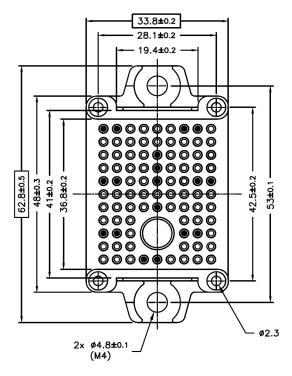


Circuit Diagram and Pin Definitions

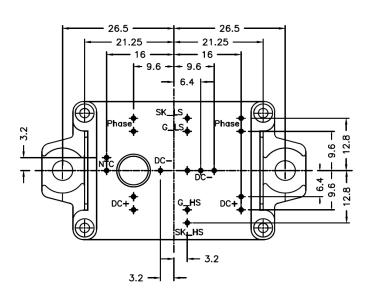








PCB HOLE PATTERN



NOTES:

- All dimensions in millimeters (mm)
 General tolerance: ± 0.1mm, unless otherwise specified













Important Mounting Information

This product is recommended for use with solder pin attach and phase change thermal interface materials, and not recommended for implementations using press fit and application of thermal grease. Please refer to mounting guidelines and user guide documents associated with this product for detailed information.

Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_G) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see https://www.qorvo.com/innovation/power-solutions/sic-power/sic-fet-design-tips.

A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the Qorvo website at https://www.qorvo.com/innovation/power-solutions/sic-power/sic-fet-design-tips.

Important notice

The information contained herein is believed to be reliable; however, Qorvo makes no warranties regarding the information contained herein and assumes no responsibility or liability whatsoever for the use of the information contained herein. All information contained herein is subject to change without notice. Customers should obtain and verify the latest relevant information before placing orders for Qorvo products. The information contained herein or any use of such information does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other intellectual property rights, whether with regard to such information itself or anything described by such information. THIS INFORMATION DOES NOT CONSTITUTE A WARRANTY WITH RESPECT TO THE PRODUCTS DESCRIBED HEREIN, AND QORVO HEREBY DISCLAIMS ANY AND ALL WARRANTIES WITH RESPECT TO SUCH PRODUCTS WHETHER EXPRESS OR IMPLIED BY LAW, COURSE OF DEALING, COURSE OF PERFORMANCE, USAGE OF TRADE OR OTHERWISE, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Without limiting the generality of the foregoing, Qorvo products are not warranted or authorized for use as critical components in medical, life-saving, or life-sustaining applications, or other applications where a failure would reasonably be expected to cause severe personal injury or death.





E1B PACKAGE OUTLINE, PART MARKING and TRAY SPECIFICATION

Table of Contents

Introduction	2
Module Package Description	
Package Outline Drawing Half Bridge Module	
Package Outline Drawing Full Brdige Module	
Branding Diagram	4
Tray	
Storage Handling	5
Storage and Handling Condition	5
ESD	5
Contact Information and Important Notice	6



Introduction

This Manufacturing Note is intended for manufacturing engineers who are currently using the module for prototype or production manufacturing. The information provided in this document is meant to assist customers with the set-up and characterization of their products.

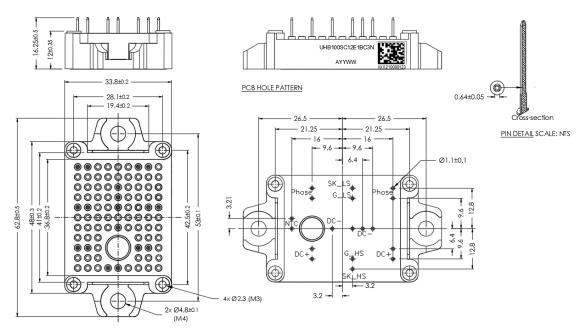
Module Package Description

This module is a SiC FET device based on a unique cascode circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's silicon-like gate-drive characteristics allows the use of unipolar gate drives, compatible with Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the E1B module package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads, and any application requiring standard gate drive Package Outline Drawing.

Package Outline Drawing

This product is recommended for use with solder pin attach and phase change thermal interface materials, and not recommended for implementations using press fit and application of thermal grease. Please refer to mounting guidelines and user guide documents associated with this product for detailed information.

Package outline for Half Bridge modules: UHB100SC12E1BC3N & UHB50SC12E1BC3N

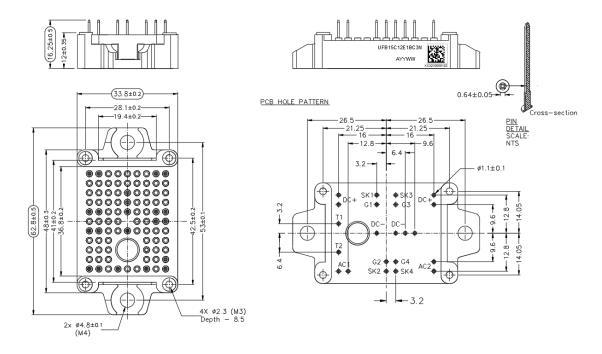


NOTES:

- 1. All dimensions in millimeters (mm)
- 2. General tolerance: ± 0.1mm, unless otherwise specified



Package outline for Full Bridge modules: UFB15C12E1BC3N & UFB25SC12E1BC3N

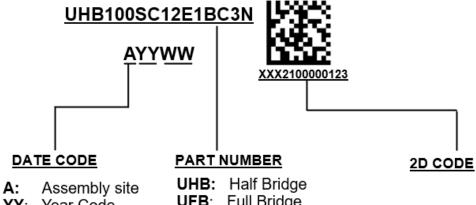


NOTES:

- 1. All dimensions in millimeters (mm)
- 2. General tolerance: \pm 0.1mm, unless otherwise specified



Branding Diagram (Marking)



YY: Year Code WW: Week Code

UFB: Full Bridge

100/50/25/15: Current rating (A)

SC/C: Stack Cascode/Cascode

12: Voltage Rating

E1B: Package Code

C3: Wafer Generation

N: NTC



Carriers

Tray and Shipping Instructions

The module is placed in an ESD tray with a pocket carrier that holds the module in dead bug orientation. The pocket is designed to hold the module for shipping and for loading onto manufacturing equipment, while protecting the body and the solder pins from damaging stresses with a lid to seal the units firmly. Then trays are placed in a shipping box with desiccant, proper label, and protective packaging so secure the tray firmly prior packing with tape.

The individual tray pocket design and count can vary from vendor to vendor.

Tray

1. Tray size and specification for large quantity

Tray size: 356x276x30 mm

Material: PS

Unit Quantity per tray: 24 pcs



Figure 1

2. Tray size and specification for small quantity

Tray size: 199x192x31 mm

Material: PS

Unit Quantity per tray: 6 pcs

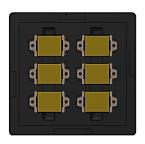




Figure 2



Storage and Handling

Storage and Handling Conditions

Excessive forces from shock or vibration as well as environmental factors must be avoided when transporting and handling the modules. Although it is not advised, it is feasible to store the modules at the temperature ranges listed in the datasheet. Furthermore, the modules can be subjected to environmental conditions, see reference below.

IEC 60721-3-1: Classification of environmental conditions.

IEC 60721- 3-2: Classification of groups of environmental parameters and their severities - Transportation and handling/

IEC 60721-3-3 Classification of groups of environmental parameters and their severities – Stationary use at weather protected locations.

ESD

Electrostatic discharge occurs naturally in the environment. With the increase in voltage potential, the outlets of neutralization or discharge will be sought. If the acquired discharge route is through a semiconductor device, destructive damage will result.

ESD countermeasure methods should be developed and used to Control potential ESD damage during handling in a factory environment at each manufacturing site.

This part is considered ESD sensitive and needs to be handled accordingly.

Qorvo recommends using standard ESD precautions (see Reference Documents) when handling these devices.

Reference Documents:

- 1. JEDEC Standard JESD625-A, "Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices."
- 2. ANSI/ESD S20.20, "Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)."

NOTE: The ESD level for this part is documented in the product qualification report that is available from Qorvo.



Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: <u>www.qorvo.com</u>
Tel: +1 833-641-3811

Email: <u>customer.support@gorvo.com</u>

Important Notice

The information contained in this Data Sheet and any associated documents ("Data Sheet Information") is believed to be reliable; however, Qorvo makes no warranties regarding the Data Sheet Information and assumes no responsibility or liability whatsoever for the use of said information. All Data Sheet Information is subject to change without notice. Customers should obtain and verify the latest relevant Data Sheet Information before placing orders for Qorvo® products. Data Sheet Information or the use thereof does not grant, explicitly, implicitly or otherwise any rights or licenses to any third party with respect to patents or any other intellectual property whether with regard to such Data Sheet Information itself or anything described by such information.

DATA SHEET INFORMATION DOES NOT CONSTITUTE A WARRANTY WITH RESPECT TO THE PRODUCTS DESCRIBED HEREIN, AND QORVO HEREBY DISCLAIMS ANY AND ALL WARRANTIES WITH RESPECT TO SUCH PRODUCTS WHETHER EXPRESS OR IMPLIED BY LAW, COURSE OF DEALING, COURSE OF PERFORMANCE, USAGE OF TRADE OR OTHERWISE, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Without limiting the generality of the foregoing, Qorvo® products are not warranted or authorized for use as critical components in medical, lifesaving, or life-sustaining applications, or other applications where a failure would reasonably be expected to cause severe personal injury or death. Applications described in the Data Sheet Information are for illustrative purposes only. Customers are responsible for validating that a particular product described in the Data Sheet Information is suitable for use in a particular application.

© 2020 Qorvo US, Inc. All rights reserved. This document is subject to copyright laws in various jurisdictions worldwide and may not be reproduced or distributed, in whole or in part, without the express written consent of Qorvo US, Inc. | QORVO® is a registered trademark of Qorvo US, Inc.

onsemi, ONSEMI., and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries. onsemi owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of onsemi's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. onsemi reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and onsemi makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems. or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

 $\textbf{Technical Library:} \ \underline{www.onsemi.com/design/resources/technical-documentation}$

onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at

www.onsemi.com/support/sales