

SiC JFET Division

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DATASHEET

J4C075060B7S

G(1)

KS (2) €













Silicon Carbide (SiC) Cascode JFET -EliteSiC, Power N-Channel, D2PAK-7L, 750 V, 58 mohm

Rev. C, January 2025

Description

The UJ4C075060B7S is a 750V, $58m\Omega$ G4 SiC FET. It is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's standard gate-drive characteristics allows for a true "drop-in replacement" to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the D²PAK-7L package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

Features

- On-resistance $R_{DS(on)}$: $58m\Omega$ (typ)
- Operating temperature: 175°C (max)
- Excellent reverse recovery: Q_{rr} = 70nC
- ◆ Low body diode V_{FSD}: 1.31V
- Low gate charge: Q_G = 37.8nC
- ◆ Threshold voltage V_{G(th)}: 4.8V (typ) allowing 0 to 15V drive
- Low intrinsic capacitance
- ESD protected, HBM class 2
- D²PAK-7L package for faster switching, clean gate waveforms
- AECQ Qualified

Package Marking D²PAK-7L UJ4C075060B7S

D (Tab)

S (3-7)



Part Number

UJ4C075060B7S

Tab





Typical applications

- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating















Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		750	V
Cata course voltage	V_{GS}	DC	-20 to +20	V
Gate-source voltage	V GS	AC (f > 1Hz)	-25 to +25	V
Continuous drain current ¹		T _C = 25°C	25.8	Α
Continuous drain current	I _D	T _C = 100°C	19	Α
Pulsed drain current ²	I _{DM}	T _C = 25°C	76	Α
Single pulsed avalanche energy ³	E _{AS}	L=15mH, I _{AS} =1.8A	24.3	mJ
SiC FET dv/dt ruggedness	dv/dt	$V_{DS} \leq 500V$	200	V/ns
Power dissipation	P _{tot}	T _C = 25°C	128	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T_J, T_{STG}		-55 to 175	°C
Reflow soldering temperature	T_{solder}	reflow MSL 1	245	°C

- 1. Limited by $T_{J,\text{max}}$
- 2. Pulse width t_p limited by $T_{J,max}$
- 3. Starting $T_J = 25^{\circ}C$

Thermal Characteristics

Darameter	Symbol	Test Conditions	Value			Units
Parameter	Symbol Test Conditi	rest Conditions	Min	Тур	Max	Offics
Thermal resistance, junction-to-case	$R_{ heta$ JC			0.9	1.17	°C/W













Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units	
Parameter	rarameter Symbol rest Condition		Min	Тур	Max	Offics	
Drain-source breakdown voltage	BV _{DS}	V_{GS} =0V, I_D =1mA	750			V	
		V _{DS} =750V,		0.7	40		
Total drain leakage current	I _{DSS}	V_{GS} =0V, T_J =25°C				μΑ	
	1033	V _{DS} =750V, V _{GS} =0V, T _J =175°C		15		μ	
Total gate leakage current	I _{GSS}	V _{DS} =0V, T _J =25°C, V _{GS} =-20V / +20V		4.7	±20	μА	
Drain-source on-resistance	R _{DS(on)}	V _{GS} =12V, I _D =20A, T _J =25°C		58	74		
		V_{GS} =12V, I_{D} =20A, T_{J} =125°C		106		mΩ	
		V_{GS} =12V, I_{D} =20A, T_{J} =175°C		147			
Gate threshold voltage	$V_{G(th)}$	V_{DS} =5V, I_{D} =10mA	4	4.8	6	V	
Gate resistance	R_{G}	f=1MHz, open drain		4.5		Ω	

Typical Performance - Reverse Diode

Davamatav	Complete T	Test Conditions	Value			I India	
Parameter	Symbol	rest Conditions	Min	Тур	Max	- Units	
Diode continuous forward current ¹	I _S	T _C =25°C			25.8	Α	
Diode pulse current ²	$I_{S,pulse}$	T _C =25°C			76	Α	
Forward voltage	V_{FSD}	V _{GS} =0V, I _F =10A, T _J =25°C		1.31	1.75	V	
Torward voltage	V FSD	V _{GS} =0V, I _F =10A, T _J =175°C		1.8		Ţ,	
Reverse recovery charge	Q_{rr}	V_R =400V, I_F =20A, V_{GS} =0V, R_{G_EXT} =20 Ω		70		nC	
Reverse recovery time	t _{rr}	di/dt=1200A/μs, Τ _J =25°C		11		ns	
Reverse recovery charge	Q_{rr}	V_R =400V, I_F =20A, V_{GS} =0V, R_{G_EXT} =20 Ω		77		nC	
Reverse recovery time	t _{rr}	di/dt=1200/μs, Τ _J =150°C		13		ns	

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D	Cll	To de Constituir de	Value			I Indian	
Parameter	Symbol	Test Conditions -	Min	Тур	Max	Units	
Input capacitance	C _{iss}	V _{DS} =400V, V _{GS} =0V		1420			
Output capacitance	C _{oss}	f=100kHz		41		pF	
Reverse transfer capacitance	C_{rss}	1-100KH2		2.7			
Effective output capacitance, energy related	C _{oss(er)}	V_{DS} =0V to 400V, V_{GS} =0V		50		pF	
Effective output capacitance, time related	C _{oss(tr)}	V_{DS} =0V to 400V, V_{GS} =0V		94		pF	
C _{OSS} stored energy	E _{oss}	V_{DS} =400V, V_{GS} =0V		4		μJ	
Total gate charge	Q_{G}	- V _{DS} =400V, I _D =20A, -		37.8			
Gate-drain charge	Q_{GD}	$V_{DS} = 400V, I_{D} = 20A,$ $V_{GS} = 0V \text{ to } 15V$		8		nC	
Gate-source charge	Q_{GS}			11.8			
Turn-on delay time	t _{d(on)}	Note 4, V_{DS} =400V, I_{D} =20A, Gate Driver =0V to +15V, Turn-on R_{GEXT} =1 Ω ,		15		- ns	
Rise time	t _r			21			
Turn-off delay time	t _{d(off)}			75			
Fall time	t _f	Turn-off $R_{G,EXT}$ =20 Ω		11			
Turn-on energy	E _{ON}	Inductive Load, - FWD: same device with		132		μ	
Turn-off energy	E _{OFF}	$V_{GS} = 0V, R_G = 20\Omega,$		29			
Total switching energy	E _{TOTAL}	T _J =25°C		161			
Turn-on delay time	t _{d(on)}	Note 4,		12			
Rise time	t _r	V _{DS} =400V, I _D =20A, Gate		23		nc	
Turn-off delay time	t _{d(off)}	$\begin{array}{c} \text{Driver = 0V to +15V,} \\ \text{Turn-on R}_{\text{G,EXT}} = 1\Omega, \\ \text{Turn-off R}_{\text{G,EXT}} = 20\Omega \end{array}$		83		ns	
Fall time	t _f			12			
Turn-on energy	E _{ON}	Inductive Load, FWD: same device with		148			
Turn-off energy	E _{OFF}	$V_{GS} = 0V, R_G = 20\Omega,$		37		μJ	
Total switching energy	E _{TOTAL}	T _J =150°C		185			

^{4.} Measured with the half-bridge mode switching test circuit in Figure 23.















Typical Performance - Dynamic (continued)

Parameter	C. mahad	Test Conditions	Value			Units
r al allietei	Symbol	rest Conditions –	Min	Тур	Max	Units
Turn-on delay time	t _{d(on)}	Notes 5 and 6,		10		
Rise time	t _r	V _{DS} =400V, I _D =20A, Gate		22		nc
Turn-off delay time	t _{d(off)}	Driver = $0V$ to + $15V$, Turn-on $R_{G,EXT} = 1\Omega$,		32		- ns
Fall time	t _f	Turn-off $R_{G,EXT} = 5\Omega$,		8		
Turn-on energy including R_{S} energy	E _{ON}	inductive Load,		96		
Turn-off energy including R_S energy	E _{OFF}	FWD: same device with V_{GS} = 0V and $R_G = 5\Omega$, RC		36		
Total switching energy	E _{TOTAL}	snubber: R_S =10 Ω and		132		μJ
Snubber R _S energy during turn-on	E _{RS_ON}	C _S =100pF, T _J =25°C		0.7		
Snubber R _S energy during turn-off	E _{RS_OFF}			1		
Turn-on delay time	t _{d(on)}	Notes 5 and 6,		14		
Rise time	t _r	V _{DS} =400V, I _D =20A, Gate		23		ns
Turn-off delay time	t _{d(off)}	Driver =0V to +15V, Turn-on $R_{G,EXT} = 1\Omega$,		45		ns
Fall time	t _f	Turn-off $R_{G,EXT} = 5\Omega$,		10		
Turn-on energy including R _S energy	E _{ON}	inductive Load,		140		
Turn-off energy including R_S energy	E _{OFF}	FWD: same device with V_{GS} = 0V and $R_G = 5\Omega$, RC		25		
Total switching energy	E _{TOTAL}	snubber: R_S =10 Ω and		165		μЈ
Snubber R _S energy during turn-on	E _{RS_ON}	C _S =100pF, T _J =150°C		0.7		1
Snubber R _S energy during turn-off	E _{RS_OFF}			1		

^{5.} Measured with the chopper mode switching test circuit in Figure 24.

^{6.} In this datasheet, all the switching energies (turn-on energy, turn-off energy and total energy) presented in the tables and Figures include the device RC snubber energy losses.







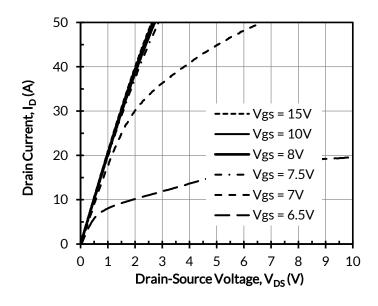








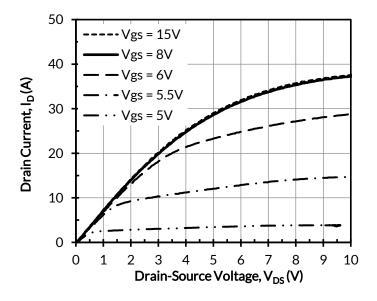
Typical Performance Diagrams



50 40 Drain Current, I_D (A) 30 Vgs = 15V 20 Vgs = 8V Vgs = 7V10 - Vgs = 6.5V -Vgs = 6V 0 0 1 2 3 10 Drain-Source Voltage, V_{DS} (V)

Figure 1. Typical output characteristics at T_J = - 55°C, tp < 250 μ s

Figure 2. Typical output characteristics at $T_J = 25$ °C, $tp < 250\mu s$



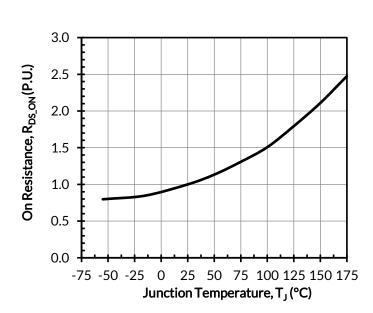


Figure 3. Typical output characteristics at T_J = 175°C, tp < 250 μ s

Figure 4. Normalized on-resistance vs. temperature at V_{GS} = 12V and I_{D} = 20A





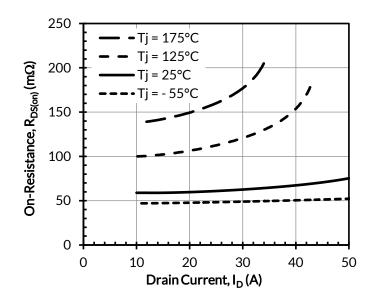












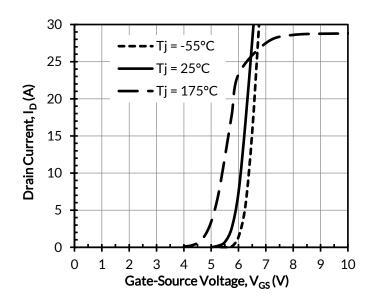
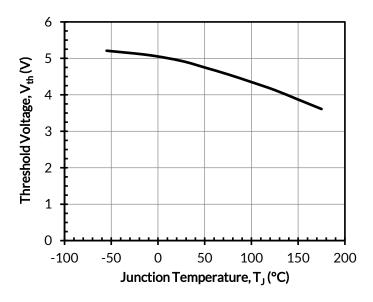


Figure 5. Typical drain-source on-resistances at V_{GS} = 12V

Figure 6. Typical transfer characteristics at V_{DS} = 5V



20 Gate-Source Voltage, V_{GS} (V) 15 10 5 ·Vds = 400V 0 -5 -10 0 10 20 30 40 50 60 Gate Charge, Q_G (nC)

Figure 7. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_{D} = 10mA

Figure 8. Typical gate charge at $I_D = 20A$





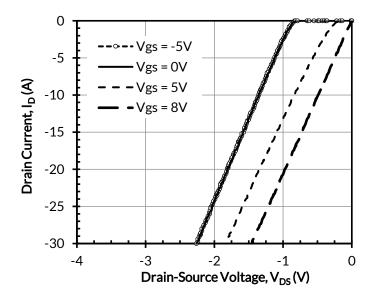








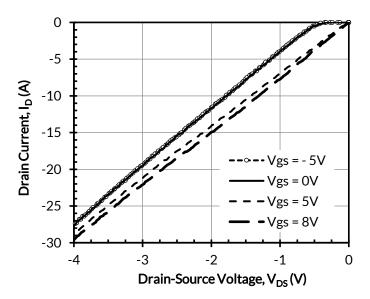




0 • Vgs = - 5V -5 Vgs = 0V Vgs = 5VDrain Current, I_D (A) -10 Vgs = 8V -15 -20 -25 -30 -3 -1 0 Drain-Source Voltage, V_{DS} (V)

Figure 9. 3rd quadrant characteristics at $T_J = -55$ °C

Figure 10. 3rd quadrant characteristics at $T_J = 25$ °C



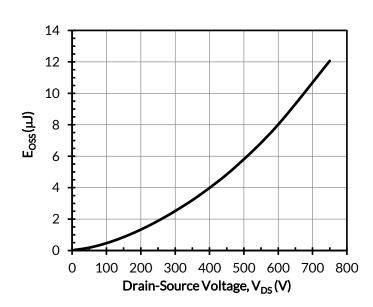


Figure 11. 3rd quadrant characteristics at $T_J = 175$ °C

Figure 12. Typical stored energy in C_{OSS} at $V_{GS} = 0V$





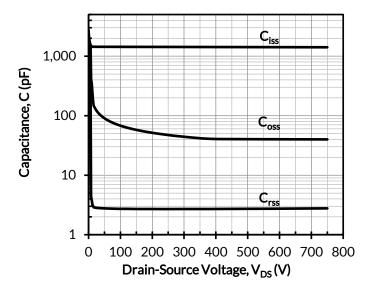








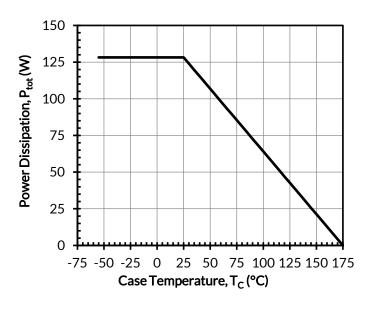




30 25 DC Drain Current, I_D (A) 20 15 10 5 0 25 50 75 100 125 150 175 -75 -50 -25 0 Case Temperature, T_C (°C)

Figure 13. Typical capacitances at f = 100kHz and V_{GS} = 0V

Figure 14. DC drain current derating



Thermal Impedance, $Z_{\theta JC}$ (°C/W) D = 0.50.1 D = 0.3**-** D = 0.1 **--** D = 0.05 0.01 ···· D = 0.02 -D = 0.01Single Pulse 0.001 1.E-06 1.E-05 1.E-04 1.E-03 1.E-02 1.E-01 Pulse Time, t_p (s)

Figure 15. Total power dissipation

Figure 16. Maximum transient thermal impedance













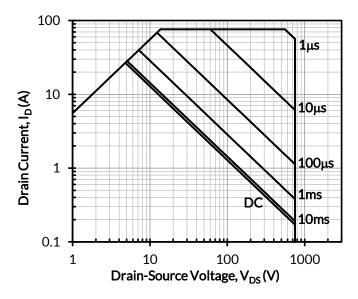


Figure 17. Safe operation area at T_C = 25°C, D = 0, Parameter t_D

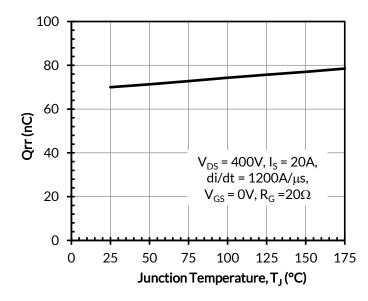


Figure 18. Reverse recovery charge Qrr vs. junction temperature

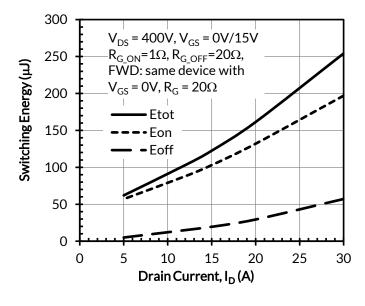


Figure 19. Clamped inductive switching energy vs. drain current at V_{DS} = 400V and T_J = 25°C

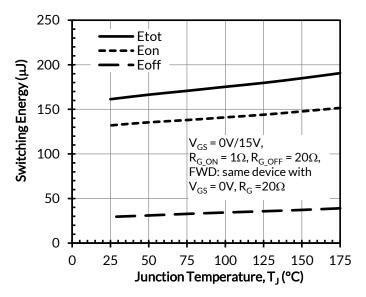


Figure 20. Clamped inductive switching energy vs. junction temperature at V_{DS} =400V and I_{D} = 20A





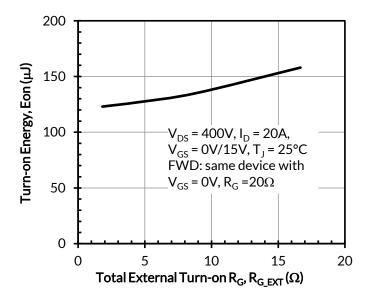








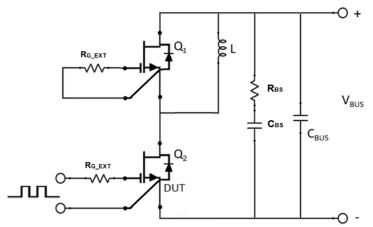




150 V_{DS} = 400V, I_{D} = 20A, V_{GS} = 0V/15V, T_{J} = 25°C FWD: same device with Turn-Off Energy, Eoff (μJ) $V_{GS} = 0V, R_G = R_{G,EXT}\Omega$ 100 50 0 0 20 40 60 80 100 Total External Turn-off R_G , $R_{G,EXT}(\Omega)$

Figure 21. Clamped inductive switching turn-on energy vs. R_{G,EXT ON}

Figure 22. Clamped inductive switching turn-off energy vs. R_{G,EXT OFF}



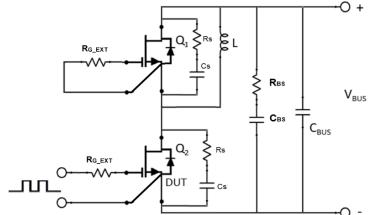


Figure 23. Schematic of the half-bridge mode switching test circuit. Note, a bus RC snubber ($R_{BS} = 2.5\Omega$, C_{BS}=100nF) is used to reduce the power loop high

Figure 24. Schematic of the half-bridge mode switching test circuit with device RC snubbers ($R_s = 10\Omega$, $C_s =$ 95pF) and a bus RC snubber ($R_{BS} = 2.5\Omega$, $C_{BS} = 100nF$).













Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode. Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.unitedsic.com.

A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the UnitedSiC website at www.unitedsic.com

Important notice

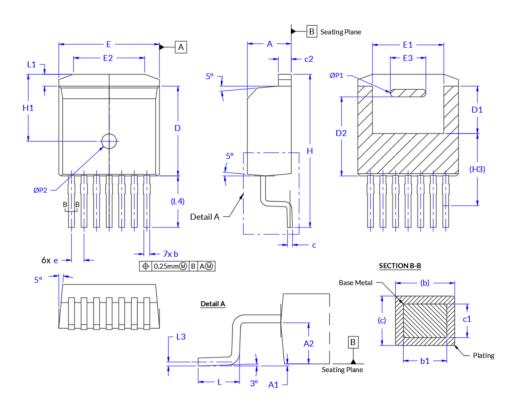
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TO263-7L (D2PAK-7L) PACKAGE OUTLINE, MARKING, TAPE AND REEL SPECIFICATION	PART	Page 1 of 4
DS TO 263 71		Rev D

PACKAGE OUTLINE



	7L-D2PAK					
SYM	М	М	IN	CH		
31141	Min	Max	Min	Max		
Α	4.30	4.56	.169	.180		
A1	0.00	0.25	.000	.010		
A2	2.45	2.75	.096	.108		
b	0.50	0.70	.020	.028		
b1	0.50	-	.020	-		
С	0.40	0.60	.016	.024		
c1	0.40		.016			
c2	1.20	1.40	.047	.055		
D	8.93	9.23	.352	.363		
D1	4.65	4.95	.183	.195		
D2	7.90	8.10	.311	.319		
e	1.27	BSC	.050 BSC			
E	10.08	10.28	.397	.405		
E1	6.82	7.62	.269	.300		
E2	6.50	8.60	.256	.339		
E3	3.50	3.70	.138	.146		
Н	15.00	16.00	.591	.630		
H1	6.68	6.88	.263	.271		
H3	7.31	REF.	.287	REF		
L	1.90	2.50	.075	.098		
L1	0.98	1.42	.039	.056		
L3	0.25	BSC	.0098	BSC		
L4	5.22	REF	.205	REF		
ØP1	0.65	0.85	.026	.033		
ØP2	1.40	1.60	.055	.063		

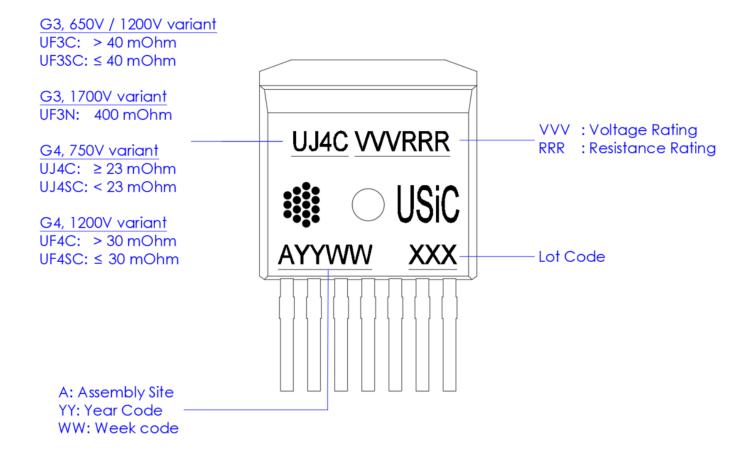
Notes:

- 1. GENERAL TOLERANCE: ±0.1 unless otherwise specified
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. PACKAGE BODY SIDES EXCLUDE MOLD FLASH AND GATE BURRS.
- 4. DIMENSION LIS MEASURED IN GAUGE LINE.
- 5. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
- 6. DIMENSION c1 AND b1 APPLIES TO BASE METAL ONLY



TO263-7L (D2PAK-7L) PACKAGE OUTLINE, PART MARKING, TAPE AND REEL SPECIFICATION	Page 2 of 4
DS_TO_263_7L	Rev D

PART MARKING



Template: FOR-000530 Rev G



TO263-7L	(D2PAK-7L)	PACKAGE	OUTLINE,	PART
MARKING,	TAPE AND RE	EL SPECIFIC	ATION	

TO 000 7

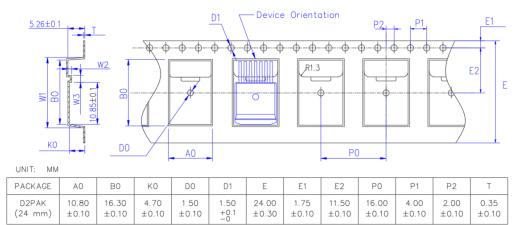
Page **3** of **4**

Rev D

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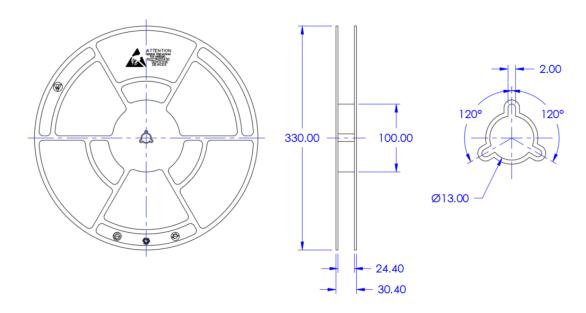
PACKING TYPE

Carrier Tape



Ext	erior	size	
	W1	16.9±0.1	
Spec	W2	1.3±0.1	
'	W3	1.0±0.1	
	W1	17.2±0.1	(1)
Spec 2	W2	1.8±0.1	(b)
	W3	0.85±0.1	0

Reel



All dimensions in millimeters Anti-Static Tape and Rell (T&R) Quantity per Reel: 800 units



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REVISION HISTORY

Revision	Create Date (mm/dd/yyyy)	Description of Change	Initiator of Change
С	11/06/2023	Updated to Qorvo template Updated Package outline drawing based latest drawing revision	Glenn Galang
D	05/21/2024	Added illustration of device orientation on carrier tape (page 3)	Glenn Galang

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