

# **SiC JFET Division**

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# Silicon Carbide (SiC) JFET - EliteSiC, Power N-Channel, TOLL, 750 V, 4.3 mohm

Rev. C, January 2025

## Description

Qorvo's UJ4N075004L8S is a 750 V,  $4.3 m\Omega$  high-performance Gen 4 normally-on SiC JFET transistor. This device exhibits ultra-low on resistance ( $R_{DS(on)}$ ) in a compact TOLL package, making it an ideal fit to address the challenging thermal and space constraints of solid-state circuit breakers and relay applications. Additionally, the JFET is a robust device technology capable of the high-energy switching required in circuit protection applications.

### **Features**

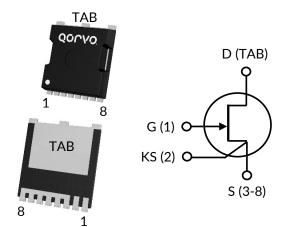
- Single digit on-resistance in a TOLL SMD package
- Operating temperature: 175°C (max)
- High pulse current capability
- Excellent device robustness
- Silver-sintered die attach for excellent thermal resistance
- · Short circuit rated
- RoHS compliant
- AECQ Qualified

# **Typical applications**

- Solid State / Semiconductor Circuit Breaker
- Solid State / Semiconductor Relay
- Battery Disconnects
- Surge Protection
- Inrush Current Control



# UJ4N075004L8S



Part Number	Package	Marking
UJ4N075004L8S	MO-229	UJ4N075004



















# **Maximum Ratings**

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	$V_{DS}$		750	V
Gate-source voltage	V	DC	-30 to +3	V
Gate-source voltage	$V_{GS}$	AC <sup>1</sup>	-30 to +30	V
Continuous drain current <sup>2</sup>	I <sub>D</sub>	T <sub>C</sub> < 145°C	120	Α
Pulsed drain current <sup>3</sup>	I <sub>DM</sub>	T <sub>C</sub> = 25°C	588	Α
Short circuit withstand time	t <sub>SC</sub>	$V_{DS} = 400V, T_{J(START)} = 175^{\circ}C$	5	μs
Power dissipation	P <sub>tot</sub>	T <sub>C</sub> = 25°C	1153	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	$T_J$ , $T_{STG}$		-55 to 175	°C
Reflow soldering temperature	$T_{solder}$	reflow MSL 1	260	°C

- 1. +30V AC rating applies for turn-on pulses <200ns applied with external  $R_{\rm G}$  >  $1\Omega.$
- 2. Limited by bondwires
- 3. Pulse width  $t_{\rm p}$  limited by  $T_{\rm J,max}$

# **Thermal Characteristics**

Parameter	Symbol Test Conditions Min	Value			Units	
raiailletei		Тур	Max	Offics		
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.10	0.13	°C/W















# Electrical Characteristics (T<sub>J</sub> = +25°C unless otherwise specified)

# **Typical Performance - Static**

Davamatar	Cymahal	Toot Conditions	Value		lue	
Parameter	Symbol	Test Conditions	Min	Тур	Max	Units
Drain-source breakdown voltage	BV <sub>DS</sub>	$V_{GS}$ =-20V, $I_D$ =2mA	750			V
		V <sub>DS</sub> =750V,		13	120	
Tabal duain la duana accument		V <sub>GS</sub> =-20V, T <sub>J</sub> =25°C				Α.
Total drain leakage current	I <sub>DSS</sub>	V <sub>DS</sub> =750V,				μΑ
		V <sub>GS</sub> =-20V, T <sub>J</sub> =175°C		65		
Total cata lackage augment		V <sub>GS</sub> =-20V, T <sub>J</sub> =25°C		0.1	100	μА
Total gate leakage current	I <sub>GSS</sub>	V <sub>GS</sub> =-20V, T <sub>J</sub> =175°C				μА
		$V_{GS}=2V, I_D=80A,$		4.0		mΩ
		T <sub>J</sub> =25°C	4.3	4.3		
		V <sub>GS</sub> =0V, I <sub>D</sub> =80A,		4.9		
Drain-source on-resistance	R <sub>DS(on)</sub>	T <sub>J</sub> =25°C			6.6	
	D5(011)	$V_{GS}=2V$ , $I_D=80A$ ,		9.9		
		T <sub>J</sub> =175°C		7.7		
		$V_{GS}$ =0V, $I_D$ =80A,	11.5			
		T <sub>J</sub> =175°C		11.5		
Gate threshold voltage	$V_{G(th)}$	$V_{DS}$ =5V, $I_D$ =180mA	-8.3	-6.0	-3.7	V
Gate resistance	$R_{G}$	f=1MHz, open drain		0.8		Ω

# Typical Performance - Dynamic

Development	Symbol Test Conditions	Value			1.1	
Parameter	Symbol	rest Conditions	Min	Тур	Max	Units
Input capacitance	$C_{iss}$	V <sub>DS</sub> =400V, V <sub>GS</sub> =-20V		3028		
Output capacitance	C <sub>oss</sub>	f=100kHz		364		pF
Reverse transfer capacitance	$C_{rss}$	I-100KHZ		360		
Effective output capacitance, energy	· ·	V <sub>DS</sub> =0V to 400V,		448		"F
related	C <sub>oss(er)</sub>	V <sub>GS</sub> =-20V		440		pF
C <sub>OSS</sub> stored energy	E <sub>oss</sub>	V <sub>DS</sub> =400V, V <sub>GS</sub> =-20V		36		μJ
Total gate charge	$Q_{G}$	\/ -400\/   -904		400		
Gate-drain charge	$Q_{GD}$	$V_{DS}$ =400V, $I_{D}$ =80A, $V_{GS}$ = -18V to 0V		270		nC
Gate-source charge	$Q_{GS}$	V <sub>GS</sub> = -18V to 0V		60		













# **Typical Performance Diagrams**

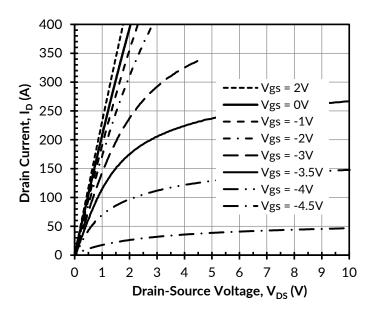


Figure 1. Typical output characteristics at  $T_J$  = - 55°C, tp < 250 $\mu$ s

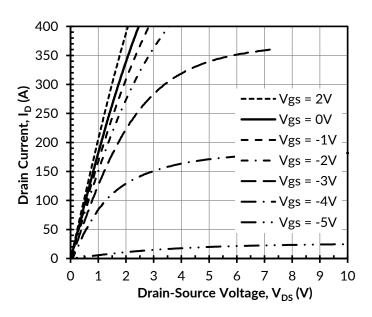


Figure 2. Typical output characteristics at  $T_J = 25$ °C, tp < 250 $\mu$ s

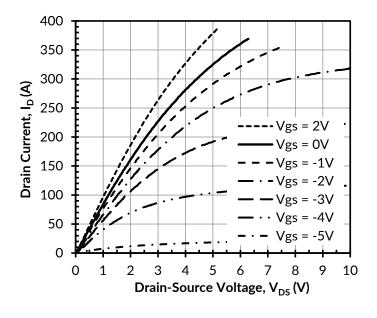


Figure 3. Typical output characteristics at  $T_J$  = 175°C, tp < 250 $\mu$ s

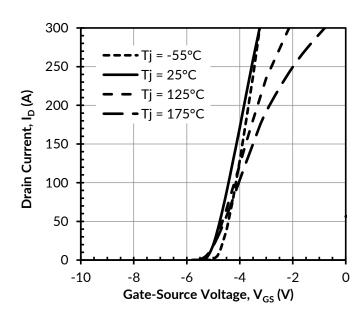


Figure 4. Typical transfer characteristics at  $V_{DS} = 5V$ 













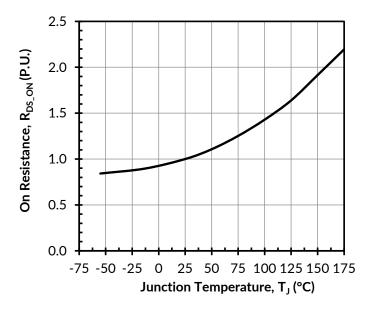
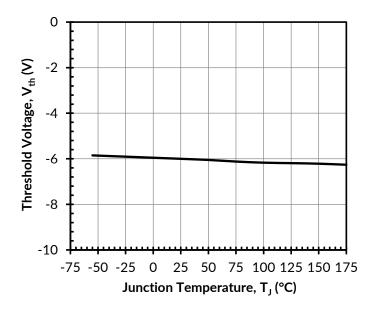


Figure 5. Normalized on-resistance vs. temperature at  $V_{GS}$  = 0V and  $I_D$  = 80A

Figure 6. Typical drain-source on-resistances at  $V_{GS} = 0V$ 



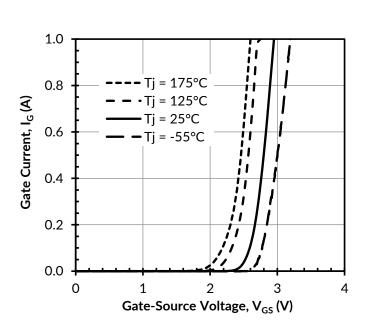


Figure 7. Threshold voltage vs. junction temperature at  $V_{DS}$  = 5V and  $I_{D}$  = 180mA

Figure 8. Typical gate forward current at  $V_{DS} = 0V$ 



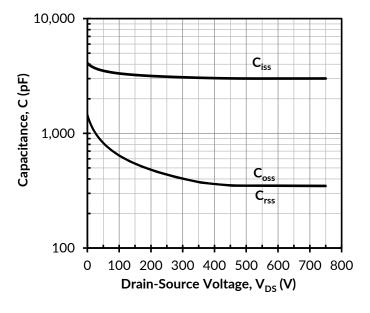








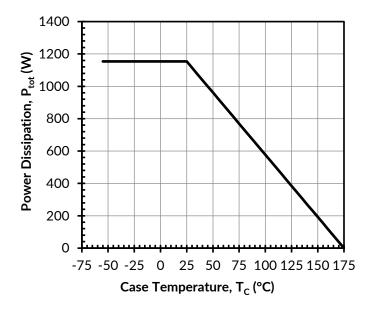




120 100 80 40 20 0 100 200 300 400 500 600 700 800 Drain-Source Voltage, V<sub>DS</sub> (V)

Figure 9. Typical capacitances at f = 100kHz and  $V_{GS} = -20V$ 

Figure 10. Typical stored energy in  $C_{OSS}$  at  $V_{GS}$  = -20V



140
120
100
80
40
20
-75 -50 -25 0 25 50 75 100 125 150 175
Case Temperature, T<sub>c</sub> (°C)

Figure 11. Total power Dissipation

Figure 12. DC drain current derating



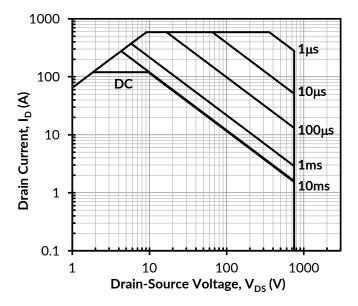












Thermal Impedance,  $Z_{\theta JC}$  (°C/W) 1.E-03 1.E-03 = 0.5 D = 0.3D = 0.1D = 0.05D = 0.02D = 0.01Single Pulse Foster model parameters Value (K/W) 2.100E-03 1.900E-03 8.000E-03 R2 5.000E-03 6.500E-02 1.400E-02 5.691E-02 4.700E-02 1.E-04 1.E-06 1.E-05 1.E-04 1.E-03 1.E-02 1.E-01 Pulse Time, t<sub>p</sub> (s)

Figure 13. Safe operation area at  $T_C$  =25°C, Parameter  $t_D$ 

Figure 14. Maximum transient thermal impedance

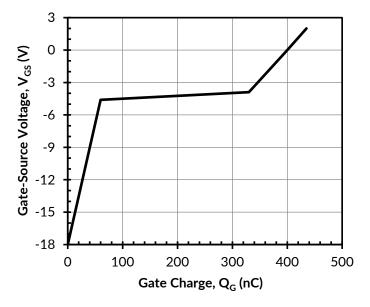


Figure 15. Typical gate charge at  $V_{DS}$  = 400V and  $I_{D}$  = 80A







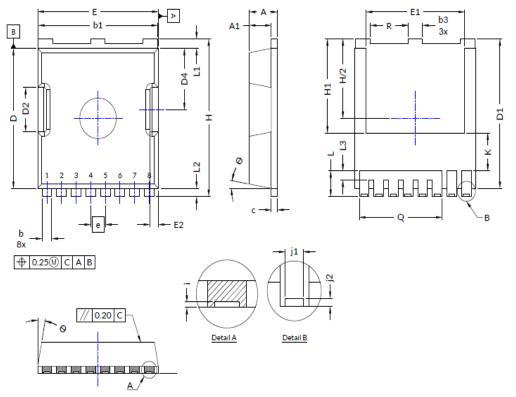








# **Package Outlines**



	TO			
TO-LL Value				
SYMBOL	Min	Nom	Max	
Α	2.15	2.30	2.45	
A1	1.80 REF			
b	0.70	0.80	0.90	
b1	9.65	9.80	9.95	
b3	1.10	1.20	1.30	
С	0.40	0.50	0.60	
D	10.18	10.38	10.58	
D1	10.98	11.08	11.18	
D2	3.15	3.30	3.45	
D4	4.40	4.55	4.70	
E	9.70	9.90	10.10	
E1	7.95	8.10	8.25	
E2	0.60	0.70	0.80	
е		1.20 BSC		
Н	11.48	11.68	11.88	
H1	6.80	6.95	7.10	
i		0.10 REF		
j1		0.46 REF		
j2		0.20 REF		
K		2.80 REF		
L	1.40	1.90	2.10	
L1	0.50	0.70	0.90	
L2	0.48	0.60	0.72	
L3	0.30	0.70	0.80	
Q		6.80 REF		
R	3.00	3.10	3.20	
θ		10°		

#### Note:

- 1. All dimensions in millimeters
- 2. Dimensions does not include Burrs and Mold Flashes
- Dimensions in compliance with JEDEC MO-299B except for backside heatsink exposed pad dimension, E1 and H1

#### Pin Designations:

- 1:Gate
- 2 : Source Kelvin
- 3-8: Source

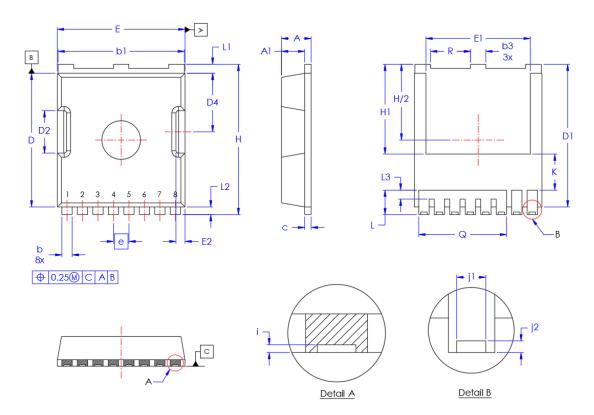
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### **PACKAGE OUTLINE**



TO-LL						
SYMBOL		Value				
	Min	Max				
A	2.15	2.45				
Al	1.80	REF				
b	0.65	0.90				
b1	9.65	9.95				
b3	1.10	1.30				
С	0.40	0.60				
D	10.18	10.58				
DI	10.88	11.28				
D2	3.15	3.45				
D4	4.40	4.70				
Е	9.70	10.10				
El	7.95	8.25				
E2	0.60 0.80					
е	1.20	BSC				
Н	11.48	11.88				
HI	6.80	7.10				
i	0.10	REF				
jl	0.46	REF				
j2	0.20	REF				
K	2.80	REF				
L	1.40	2.10				
L1	0.50	0.90				
L2	0.48	0.72				
L3	0.30	0.80				
Q	6.80 REF					
R	3.00	3 20				

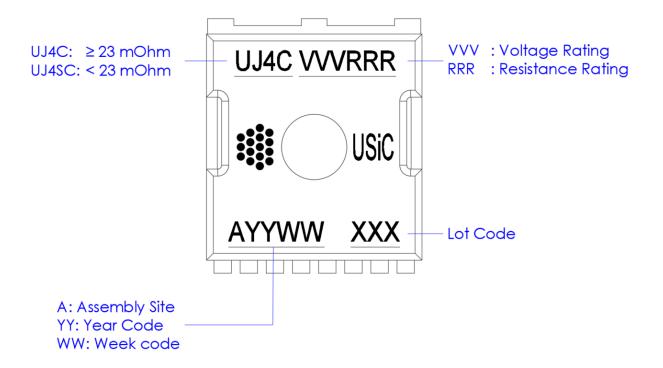
### Note:

- 1. All dimensions in millimeters
- 2. Dimensions does not include Burrs and Mold Flashes



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#### **PART MARKING**



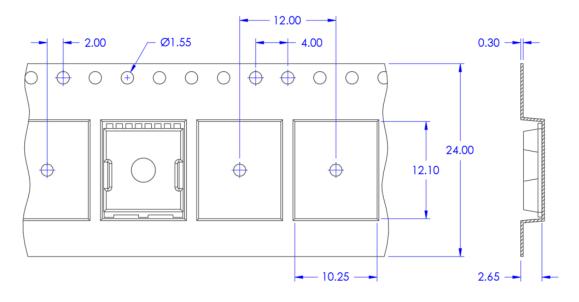
Template: FOR-000530 Rev G



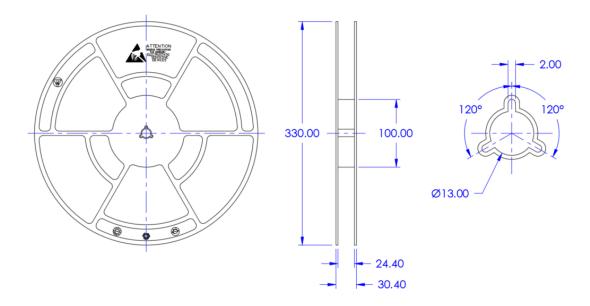
TOLL PACKAGE OUTLINE, PART MARKING, TAPE AND REEL SPECIFICATION	Page 3 of 4
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### **PACKING TYPE**

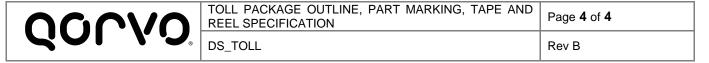
### Carrier Tape



### Reel



All dimensions in millimeters Quantity per Reel: 2000 units



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#### **REVISION HISTORY**

Revision	Create Date (mm/dd/yyyy)	Description of Change	Initiator of Change
Α	10/13/2023	Initial Production Release	Glenn Galang
В	01/31/2024	Corrected device orientation inside carrier tape pocket (Page 3)	Glenn Galang

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