

QORVO

SiC JFET Division

Is Now Part of

onsemi™

To learn more about onsemi™, please visit our website at
www.onsemi.com

onsemi and **onsemi** and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi** product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner. Other names and brands may be claimed as the property of others.

Silicon Carbide (SiC) Cascode JFET - EliteSiC, Power N-Channel, D²PAK-7L, 750V, 9 mohm

Rev. B, January 2025

DATASHEET

UJ4SC075009B7S

Description

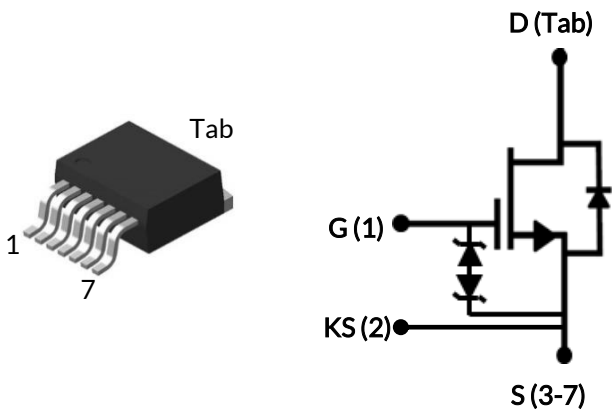
The UJ4SC075009B7S is a 750V, 9mΩ G4 SiC FET. It is based on a unique ‘cascode’ circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device’s standard gate-drive characteristics allows for a true “drop-in replacement” to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the D²PAK-7L package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

Features

- ◆ On-resistance $R_{DS(on)}$: 9mΩ (typ)
- ◆ Operating temperature: 175°C (max)
- ◆ Excellent reverse recovery: Q_{rr} = 338nC
- ◆ Low body diode V_{FSD} : 1.1V
- ◆ Low gate charge: Q_G = 75nC
- ◆ Threshold voltage $V_{G(th)}$: 4.5V (typ) allowing 0 to 15V drive
- ◆ Low intrinsic capacitance
- ◆ ESD protected, HBM class 2
- ◆ D²PAK-7L package for faster switching, clean gate waveforms
- ◆ AECQ Qualified

Typical applications

- ◆ EV charging
- ◆ PV inverters
- ◆ Switch mode power supplies
- ◆ Power factor correction modules
- ◆ Motor drives
- ◆ Induction heating



Part Number	Package	Marking
UJ4SC075009B7S	D ² PAK-7L	UJ4SC075009B7S



Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		750	V
Gate-source voltage	V_{GS}	DC	-20 to +20	V
		AC (f > 1Hz)	-25 to +25	V
Continuous drain current ¹	I_D	$T_C < 61^\circ\text{C}$	106	A
		$T_C = 100^\circ\text{C}$	86	A
Pulsed drain current ²	I_{DM}	$T_C = 25^\circ\text{C}$	344	A
Single pulsed avalanche energy ³	E_{AS}	L=15mH, $I_{AS} = 5.2\text{A}$	202	mJ
SiC FET dv/dt ruggedness	dv/dt	$V_{DS} \leq 500\text{V}$	100	V/ns
Power dissipation	P_{tot}	$T_C = 25^\circ\text{C}$	375	W
Maximum junction temperature	$T_{J,max}$		175	$^\circ\text{C}$
Operating and storage temperature	T_J, T_{STG}		-55 to 175	$^\circ\text{C}$
Reflow soldering temperature	T_{solder}	reflow MSL 1	245	$^\circ\text{C}$

- Limited by bondwires
- Pulse width t_p limited by $T_{J,max}$
- Starting $T_J = 25^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.31	0.40	$^\circ\text{C/W}$

Electrical Characteristics ($T_J = +25^\circ\text{C}$ unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	$V_{GS}=0V, I_D=1mA$	750			V
Total drain leakage current	I_{DSS}	$V_{DS}=750V, V_{GS}=0V, T_J=25^\circ\text{C}$		4	84	μA
		$V_{DS}=750V, V_{GS}=0V, T_J=175^\circ\text{C}$		35		
Total gate leakage current	I_{GSS}	$V_{DS}=0V, T_J=25^\circ\text{C}, V_{GS}=-20V / +20V$		2	± 20	μA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=12V, I_D=70A, T_J=25^\circ\text{C}$		9	11.5	m Ω
		$V_{GS}=12V, I_D=70A, T_J=125^\circ\text{C}$		14.8		
		$V_{GS}=12V, I_D=70A, T_J=175^\circ\text{C}$		19.4		
Gate threshold voltage	$V_{G(th)}$	$V_{DS}=5V, I_D=10mA$	3.5	4.5	5.5	V
Gate resistance	R_G	f=1MHz, open drain		2.3		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current ¹	I_S	$T_C < 61^\circ\text{C}$			106	A
Diode pulse current ²	$I_{S,pulse}$	$T_C=25^\circ\text{C}$			344	A
Forward voltage	V_{FSD}	$V_{GS}=0V, I_F=35A, T_J=25^\circ\text{C}$		1.10	1.24	V
		$V_{GS}=0V, I_F=35A, T_J=175^\circ\text{C}$		1.14		
Reverse recovery charge	Q_{rr}	$V_R=400V, I_F=70A, V_{GS}=0V, R_{G,EXT}=33\Omega, di/dt=2500A/\mu\text{s}, T_J=25^\circ\text{C}$		338		nC
Reverse recovery time	t_{rr}	$T_J=25^\circ\text{C}$		29		ns
Reverse recovery charge	Q_{rr}	$V_R=400V, I_F=70A, V_{GS}=0V, R_{G,EXT}=33\Omega, di/dt=2500A/\mu\text{s}, T_J=150^\circ\text{C}$		375		nC
Reverse recovery time	t_{rr}	$T_J=150^\circ\text{C}$		32		ns

Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	$V_{DS}=400V, V_{GS}=0V$ $f=100kHz$		3340		pF
Output capacitance	C_{oss}			230		
Reverse transfer capacitance	C_{rss}			1.4		
Effective output capacitance, energy related	$C_{oss(er)}$	$V_{DS}=0V$ to 400V, $V_{GS}=0V$		286		pF
Effective output capacitance, time related	$C_{oss(tr)}$	$V_{DS}=0V$ to 400V, $V_{GS}=0V$		605		pF
C_{OSS} stored energy	E_{oss}	$V_{DS}=400V, V_{GS}=0V$		23		μJ
Total gate charge	Q_G	$V_{DS}=400V, I_D=70A,$ $V_{GS} = 0V$ to 15V		75		nC
Gate-drain charge	Q_{GD}			13		
Gate-source charge	Q_{GS}			22		
Turn-on delay time	$t_{d(on)}$	Notes 4 and 5, $V_{DS}=400V, I_D=70A,$ Gate Driver =0V to +15V, Turn-on $R_{G,EXT}=1\Omega,$ Turn-off $R_{G,EXT}=5\Omega,$ inductive Load, FWD: same device with $V_{GS} = 0V$ and $R_G = 5\Omega,$ RC snubber: $R_S=5\Omega$ and $C_S=560pF,$ $T_J=25^\circ C$		17		ns
Rise time	t_r			25		
Turn-off delay time	$t_{d(off)}$			65		
Fall time	t_f			14		
Turn-on energy including R_S energy	E_{ON}			220		
Turn-off energy including R_S energy	E_{OFF}	Notes 4 and 5, $V_{DS}=400V, I_D=70A,$ Gate Driver =0V to +15V, Turn-on $R_{G,EXT}=1\Omega,$ Turn-off $R_{G,EXT}=5\Omega,$ inductive Load, FWD: same device with $V_{GS} = 0V$ and $R_G = 5\Omega,$ RC snubber: $R_S=5\Omega$ and $C_S=560pF,$ $T_J=150^\circ C$		181		μJ
Total switching energy	E_{TOTAL}			401		
Snubber R_S energy during turn-on	E_{RS_ON}			13		
Snubber R_S energy during turn-off	E_{RS_OFF}			50		
Turn-on delay time	$t_{d(on)}$			18		
Rise time	t_r	Notes 4 and 5, $V_{DS}=400V, I_D=70A,$ Gate Driver =0V to +15V, Turn-on $R_{G,EXT}=1\Omega,$ Turn-off $R_{G,EXT}=5\Omega,$ inductive Load, FWD: same device with $V_{GS} = 0V$ and $R_G = 5\Omega,$ RC snubber: $R_S=5\Omega$ and $C_S=560pF,$ $T_J=150^\circ C$		28		ns
Turn-off delay time	$t_{d(off)}$			68		
Fall time	t_f			13		
Turn-on energy including R_S energy	E_{ON}			245		
Turn-off energy including R_S energy	E_{OFF}			211		
Total switching energy	E_{TOTAL}	Notes 4 and 5, $V_{DS}=400V, I_D=70A,$ Gate Driver =0V to +15V, Turn-on $R_{G,EXT}=1\Omega,$ Turn-off $R_{G,EXT}=5\Omega,$ inductive Load, FWD: same device with $V_{GS} = 0V$ and $R_G = 5\Omega,$ RC snubber: $R_S=5\Omega$ and $C_S=560pF,$ $T_J=150^\circ C$		456		μJ
Snubber R_S energy during turn-on	E_{RS_ON}			13		
Snubber R_S energy during turn-off	E_{RS_OFF}			50		

4. Measured with the switching test circuit in Figure 26.

5. In this datasheet, all the switching energies (turn-on energy, turn-off energy and total energy) presented in the tables and Figures include the device RC snubber energy losses.

Typical Performance Diagrams

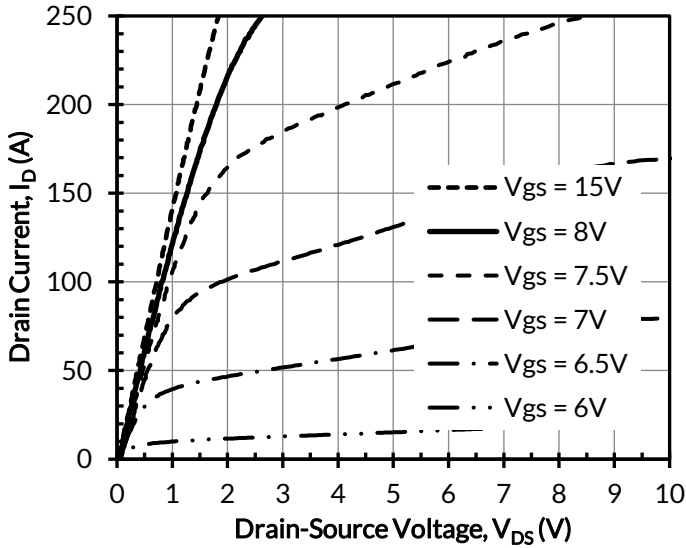


Figure 1. Typical output characteristics at $T_j = -55^\circ\text{C}$, $t_p < 250\mu\text{s}$

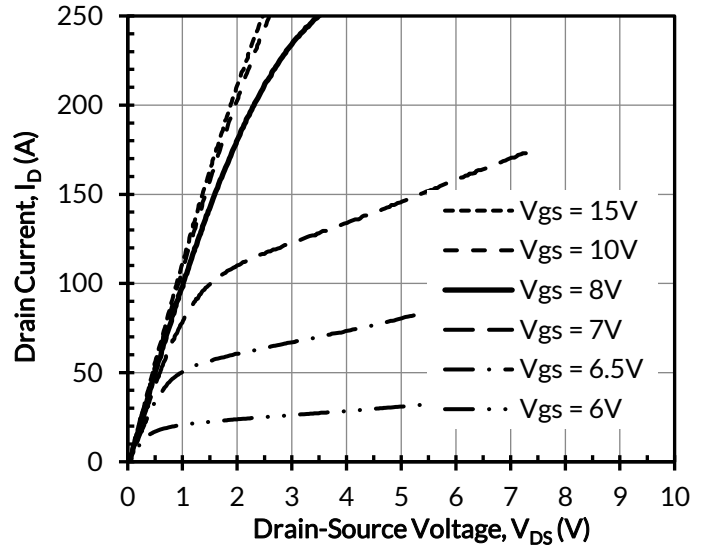


Figure 2. Typical output characteristics at $T_j = 25^\circ\text{C}$, $t_p < 250\mu\text{s}$

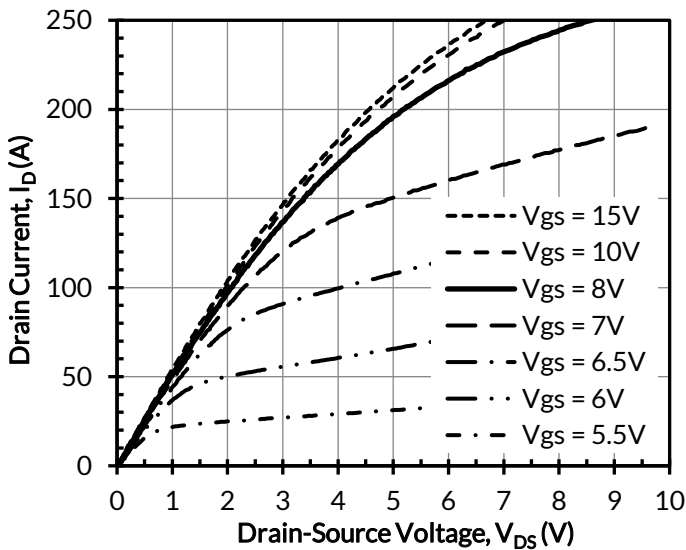


Figure 3. Typical output characteristics at $T_j = 175^\circ\text{C}$, $t_p < 250\mu\text{s}$

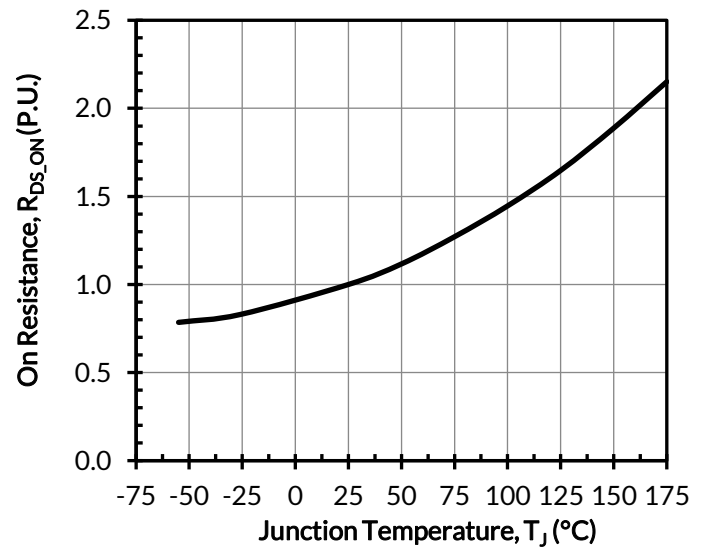


Figure 4. Normalized on-resistance vs. temperature at $V_{GS} = 12\text{V}$ and $I_D = 70\text{A}$

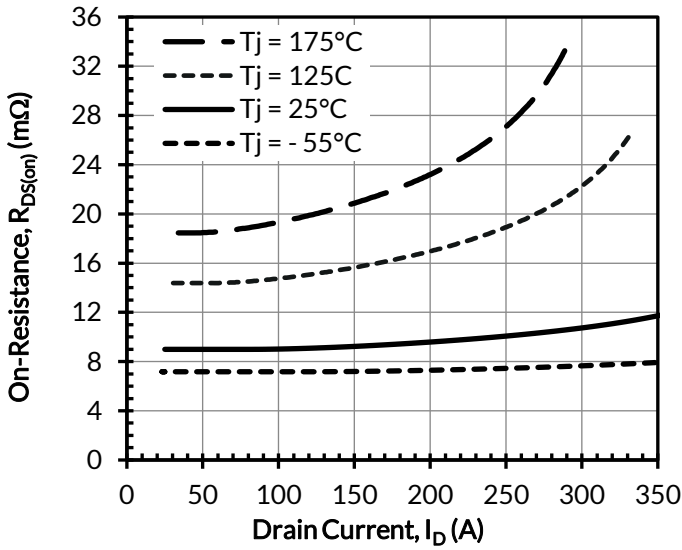


Figure 5. Typical drain-source on-resistances at $V_{GS} = 12V$

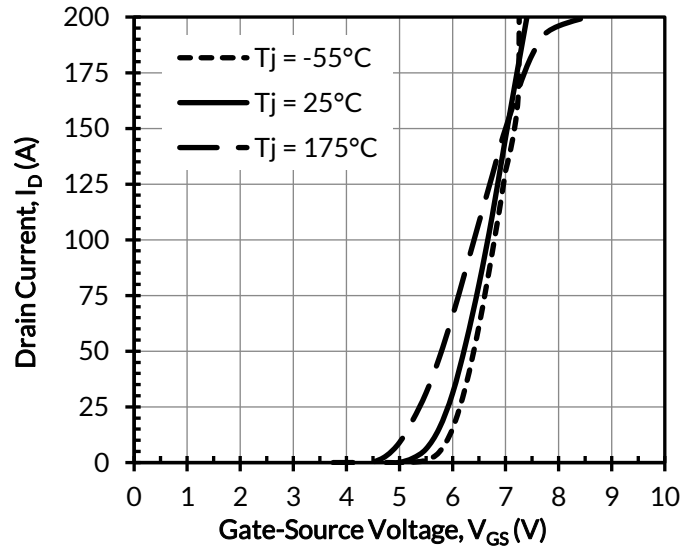


Figure 6. Typical transfer characteristics at $V_{DS} = 5V$

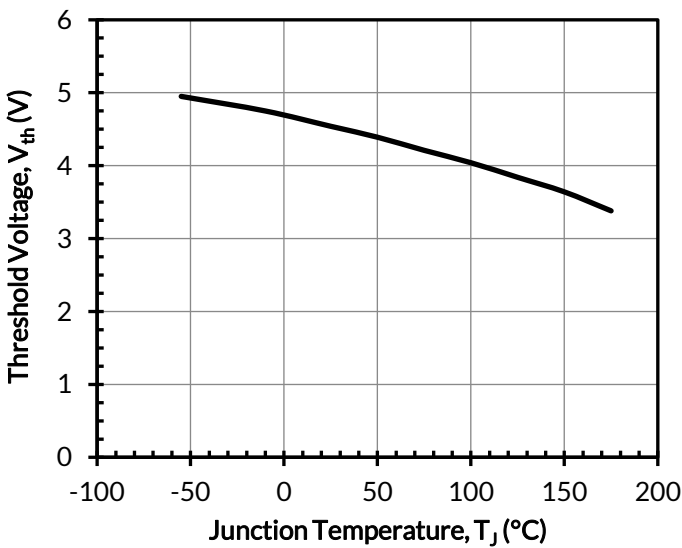


Figure 7. Threshold voltage vs. junction temperature at $V_{DS} = 5V$ and $I_D = 10mA$

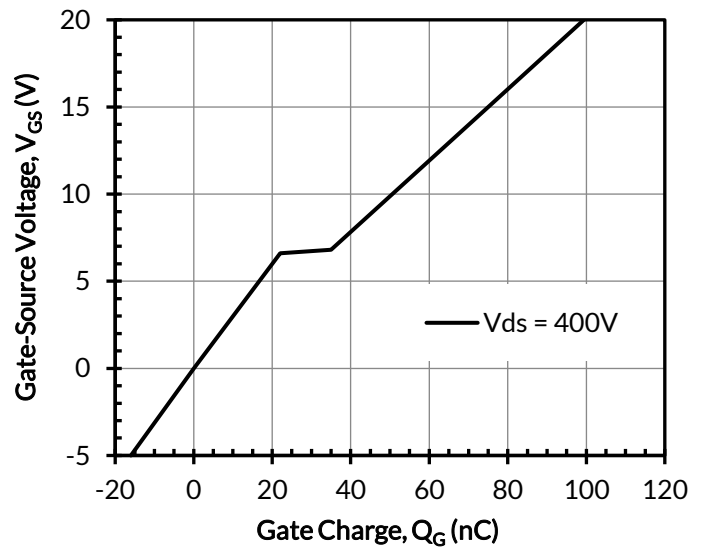


Figure 8. Typical gate charge at $I_D = 70A$

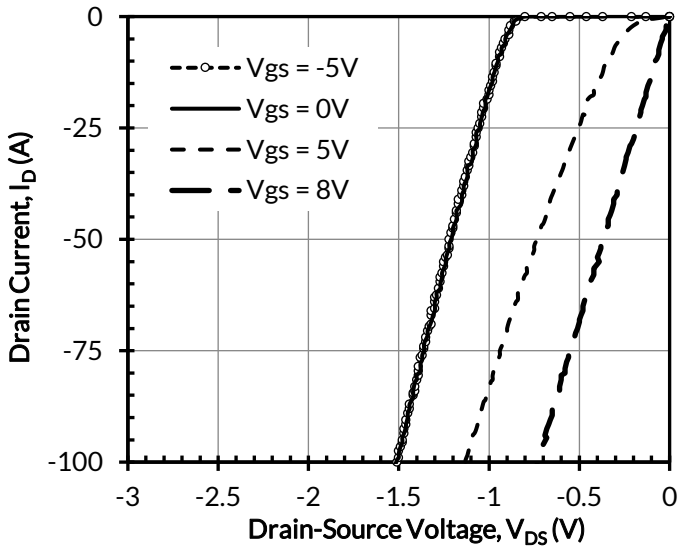


Figure 9. 3rd quadrant characteristics at $T_j = -55^\circ\text{C}$

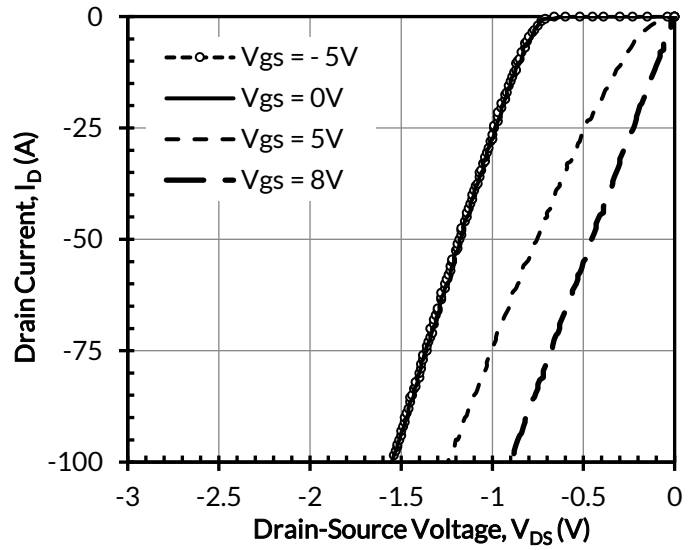


Figure 10. 3rd quadrant characteristics at $T_j = 25^\circ\text{C}$

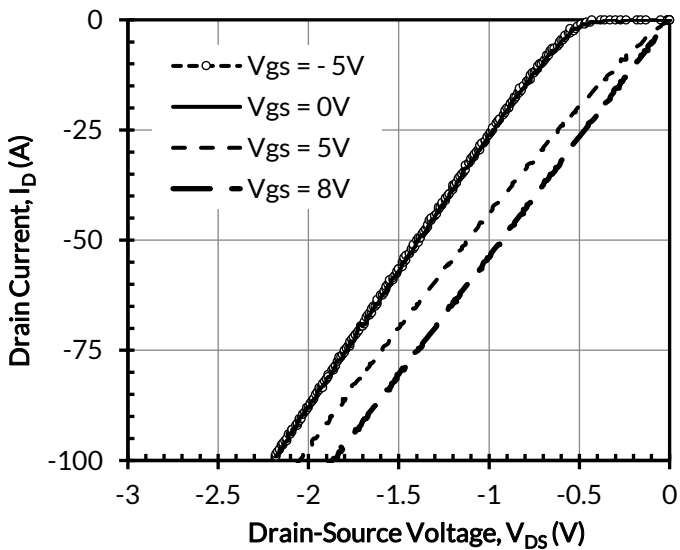


Figure 11. 3rd quadrant characteristics at $T_j = 175^\circ\text{C}$

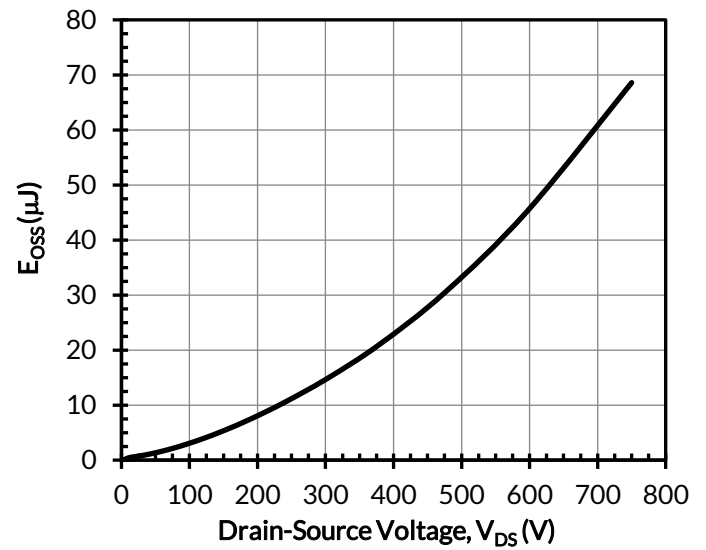


Figure 12. Typical stored energy in C_{OSS} at $V_{GS} = 0\text{V}$

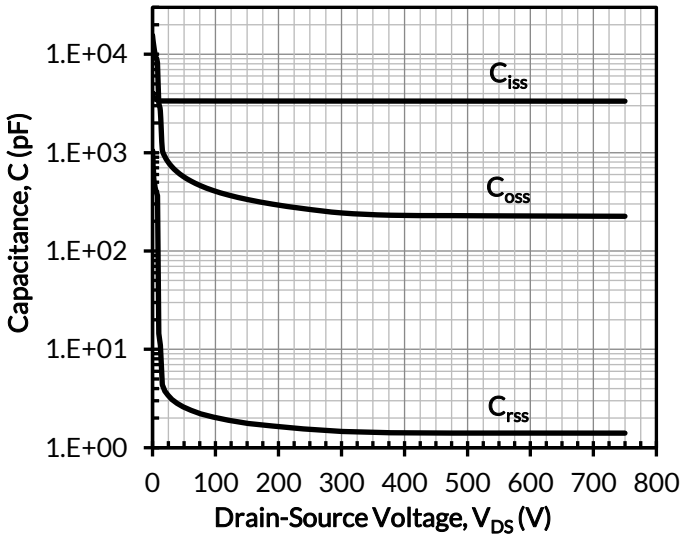


Figure 13. Typical capacitances at $f = 100\text{kHz}$ and $V_{GS} = 0\text{V}$

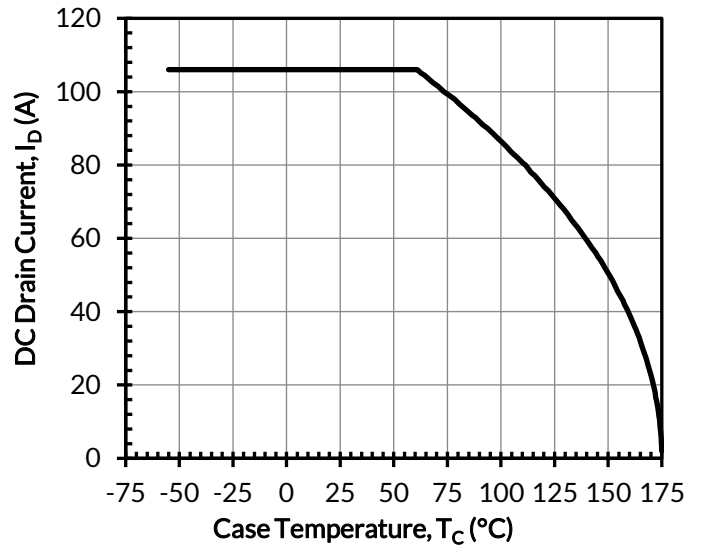


Figure 14. DC drain current derating

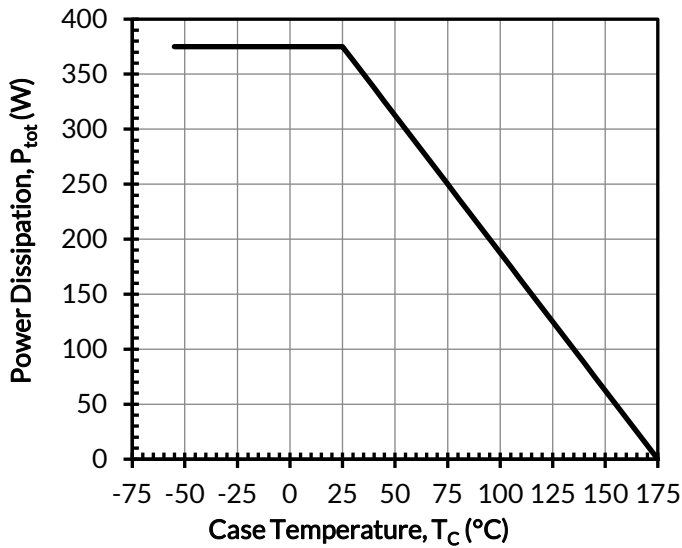


Figure 15. Total power dissipation

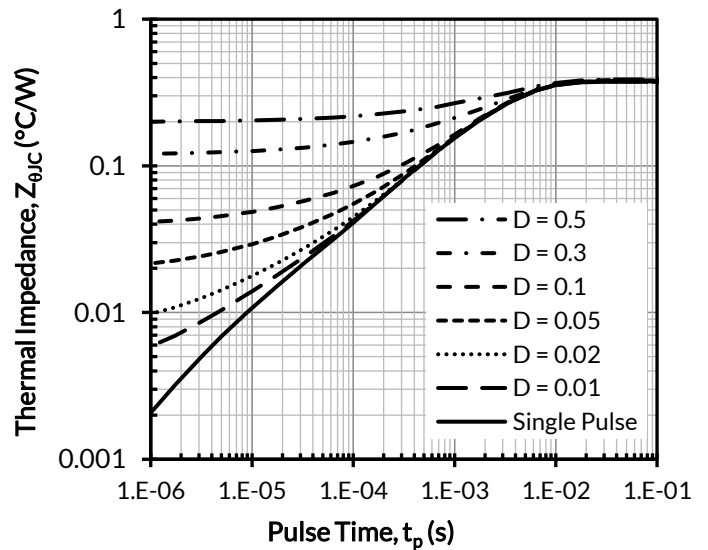


Figure 16. Maximum transient thermal impedance

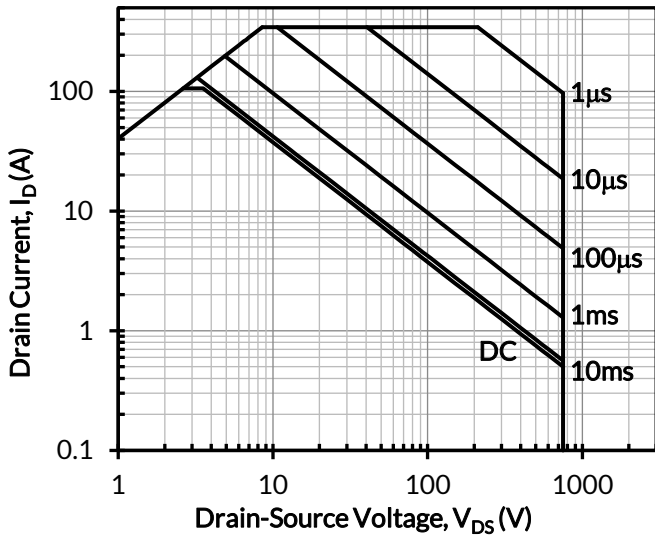


Figure 17. Safe operation area at $T_C = 25^\circ\text{C}$, $D = 0$, Parameter t_p

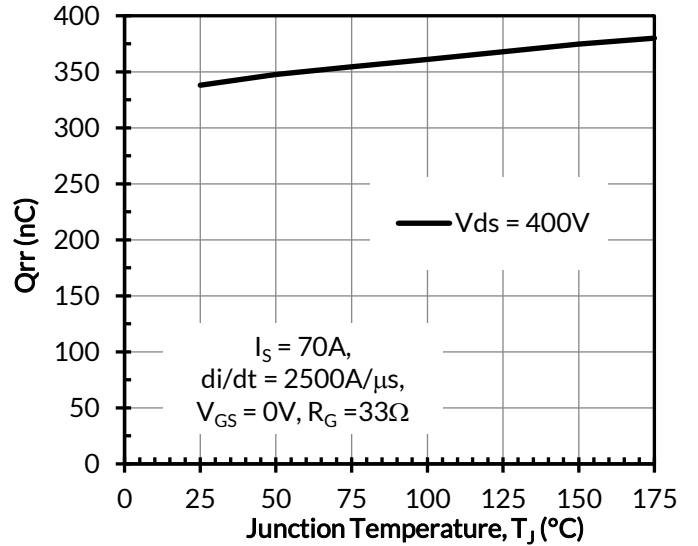


Figure 18. Reverse recovery charge Q_{rr} vs. junction temperature

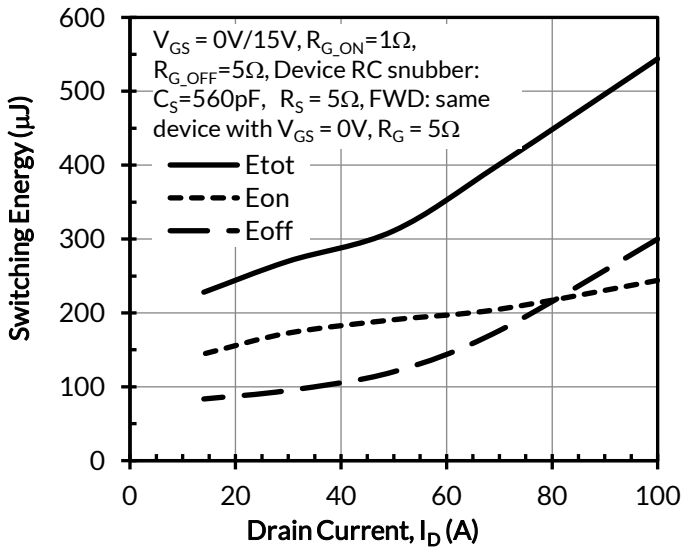


Figure 19. Clamped inductive switching energy vs. drain current at $V_{DS} = 400\text{V}$ and $T_J = 25^\circ\text{C}$

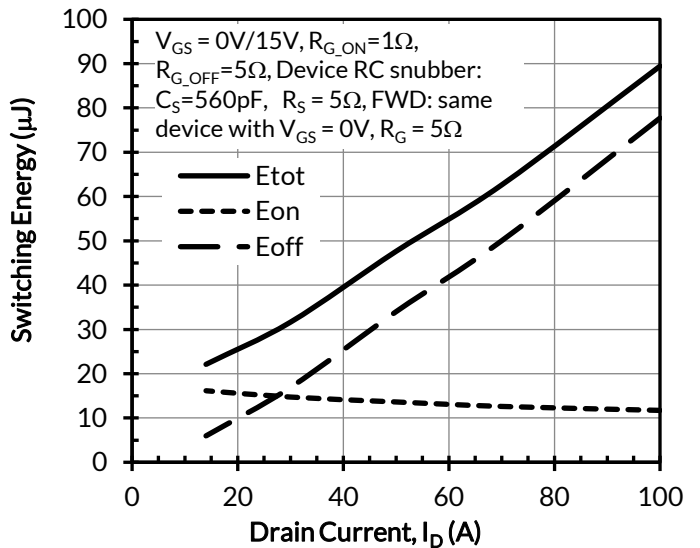


Figure 20. RC snubber energy loss vs. drain current at $V_{DS} = 400\text{V}$ and $T_J = 25^\circ\text{C}$

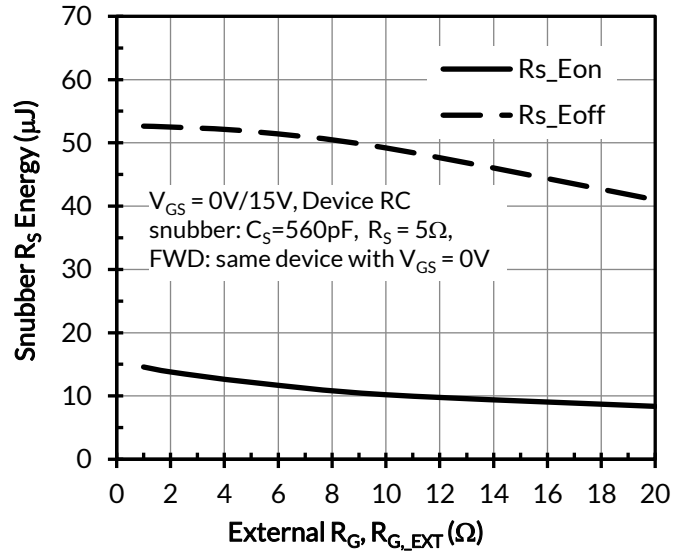
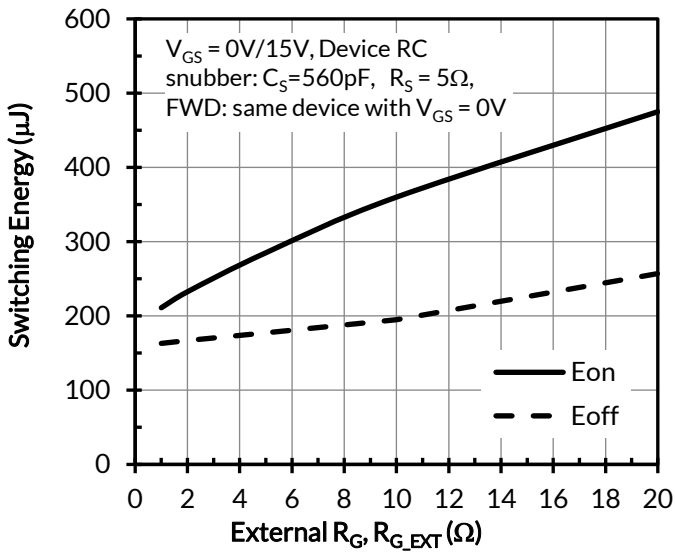


Figure 21. Clamped inductive switching energy vs. $R_{G,EXT}$ at $V_{DS} = 400V$, $I_D = 70A$, and $T_J = 25^\circ C$

Figure 22. RC snubber energy losses vs. $R_{G,EXT}$ at $V_{DS} = 400V$, $I_D = 70A$, and $T_J = 25^\circ C$

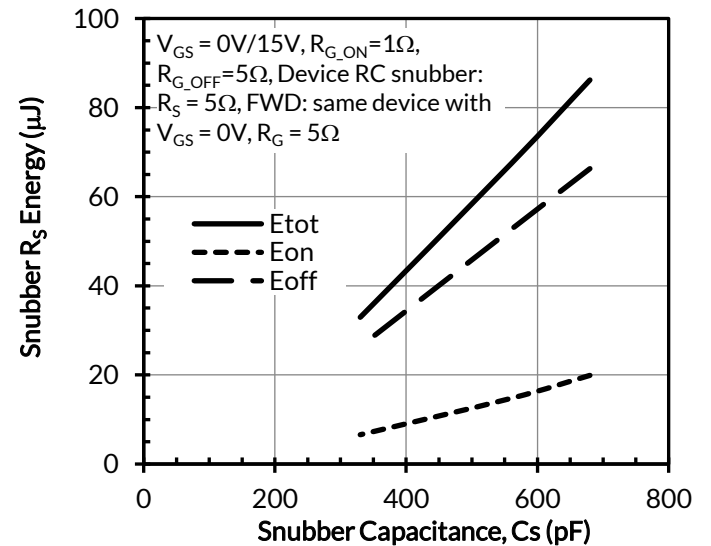
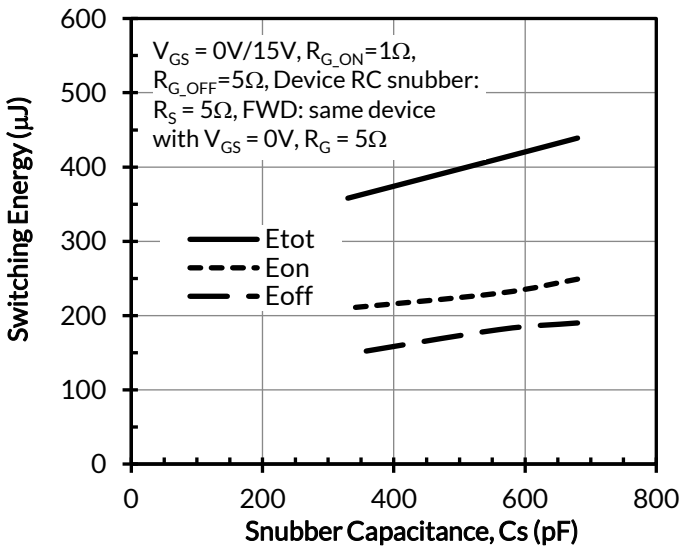


Figure 23. Clamped inductive switching energy vs. Snubber Capacitance C_S at $V_{DS} = 400V$, $I_D = 70A$, and $T_J = 25^\circ C$

Figure 24. RC snubber energy loss vs. Snubber Capacitance C_S at $V_{DS} = 400V$, $I_D = 70A$, and $T_J = 25^\circ C$

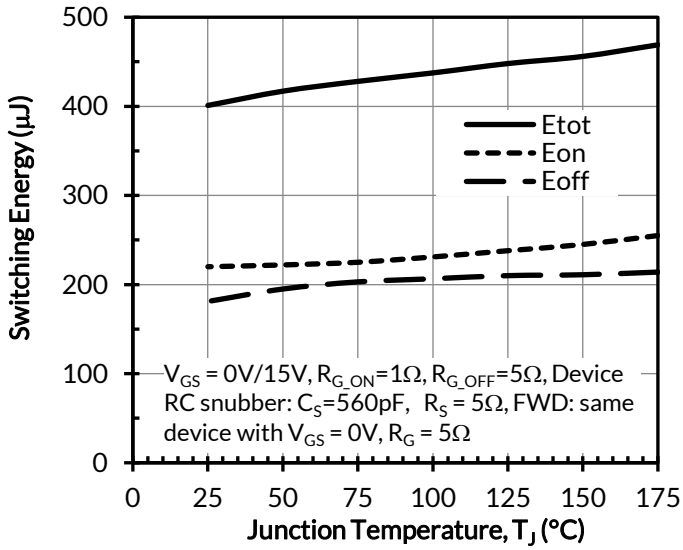


Figure 25. Clamped inductive switching energies vs. junction temperature T_J at $V_{DS} = 400V$, and $I_D = 70A$

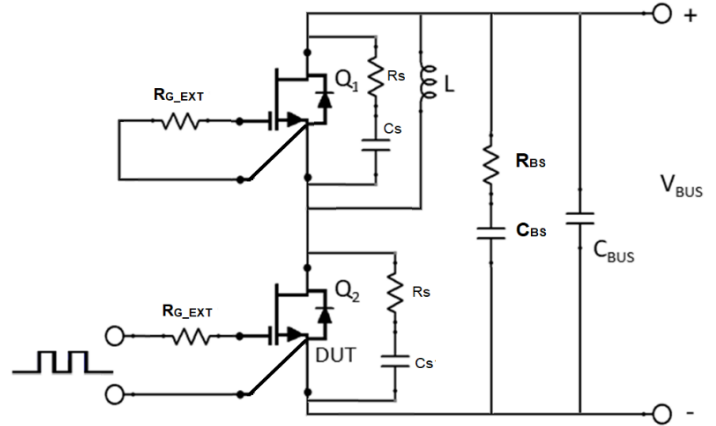


Figure 26. Schematic of the half-bridge mode switching test circuit. Note, a bus RC snubber ($R_{BS} = 1\Omega$, $C_{BS} = 100nF$) is used to reduce the power loop high frequency oscillations.

Applications Information

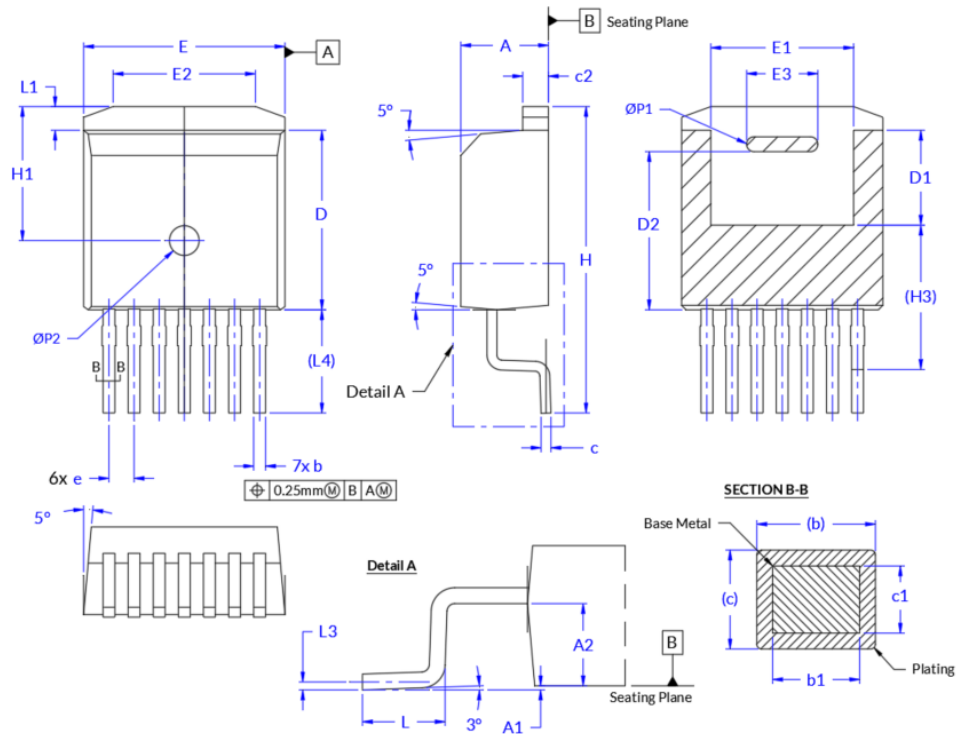
SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.unitedsic.com.

A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the UnitedSiC website at www.unitedsic.com

Important notice

The information contained herein is believed to be reliable; however, Qorvo makes no warranties regarding the information contained herein and assumes no responsibility or liability whatsoever for the use of the information contained herein. All information contained herein is subject to change without notice. Customers should obtain and verify the latest relevant information before placing orders for Qorvo products. The information contained herein or any use of such information does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other intellectual property rights, whether with regard to such information itself or anything described by such information. THIS INFORMATION DOES NOT CONSTITUTE A WARRANTY WITH RESPECT TO THE PRODUCTS DESCRIBED HEREIN, AND QORVO HEREBY DISCLAIMS ANY AND ALL WARRANTIES WITH RESPECT TO SUCH PRODUCTS WHETHER EXPRESS OR IMPLIED BY LAW, COURSE OF DEALING, COURSE OF PERFORMANCE, USAGE OF TRADE OR OTHERWISE, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Without limiting the generality of the foregoing, Qorvo products are not warranted or authorized for use as critical components in medical, life-saving, or life-sustaining applications, or other applications where a failure would reasonably be expected to cause severe personal injury or death.

PACKAGE OUTLINE


SYM	7L-D2PAK			
	MM		MIN	MAX
A	4.30	4.56	.169	.180
A1	0.00	0.25	.000	.010
A2	2.45	2.75	.096	.108
b	0.50	0.70	.020	.028
b1	0.50	-	.020	-
c	0.40	0.60	.016	.024
c1	0.40	-	.016	-
c2	1.20	1.40	.047	.055
D	8.93	9.23	.352	.363
D1	4.65	4.95	.183	.195
D2	7.90	8.10	.311	.319
e	1.27 BSC		.050 BSC	
E	10.08	10.28	.397	.405
E1	6.82	7.62	.269	.300
E2	6.50	8.60	.256	.339
E3	3.50	3.70	.138	.146
H	15.00	16.00	.591	.630
H1	6.68	6.88	.263	.271
H3	7.3 REF.		.287 REF	
L	1.90	2.50	.075	.098
L1	0.98	1.42	.039	.056
L3	0.25 BSC		.0098 BSC	
L4	5.22 REF		.205 REF	
ØP1	0.65	0.85	.026	.033
ØP2	1.40	1.60	.055	.063

Notes:

1. GENERAL TOLERANCE: ± 0.1 unless otherwise specified
2. CONTROLLING DIMENSION: **MILLIMETERS**
3. PACKAGE BODY SIDES EXCLUDE MOLD FLASH AND GATE BURRS.
4. DIMENSION L IS MEASURED IN GAUGE LINE.
5. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
6. DIMENSION c1 AND b1 APPLIES TO BASE METAL ONLY

PART MARKING

G3, 650V / 1200V variant

UF3C: > 40 mOhm

UF3SC: ≤ 40 mOhm

G3, 1700V variant

UF3N: 400 mOhm

G4, 750V variant

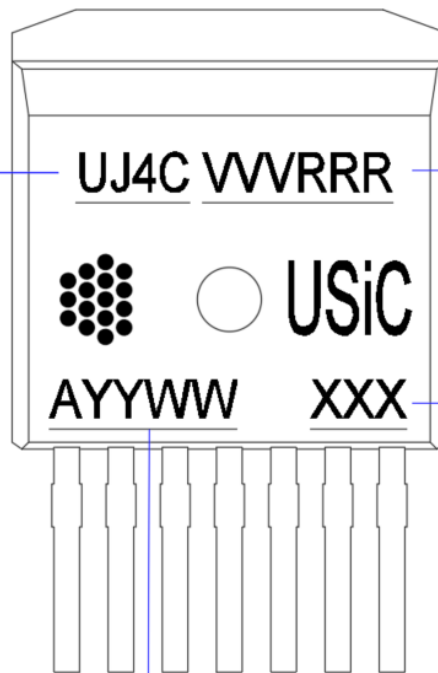
UJ4C: ≥ 23 mOhm

UJ4SC: < 23 mOhm

G4, 1200V variant

UF4C: > 30 mOhm

UF4SC: ≤ 30 mOhm



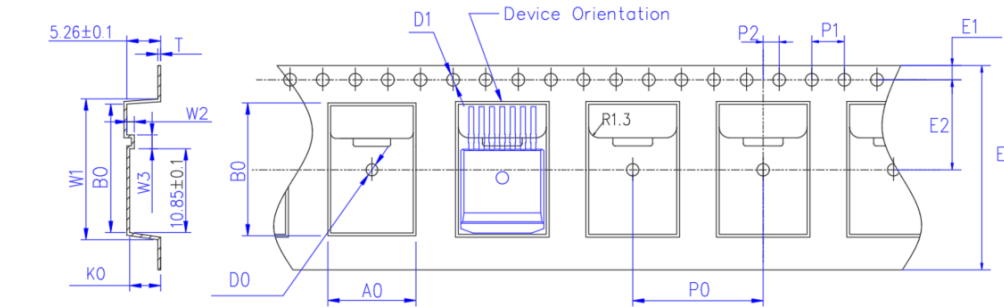
VVV : Voltage Rating
 RRR : Resistance Rating

Lot Code

A: Assembly Site
 YY: Year Code
 WW: Week code

PACKING TYPE

Carrier Tape

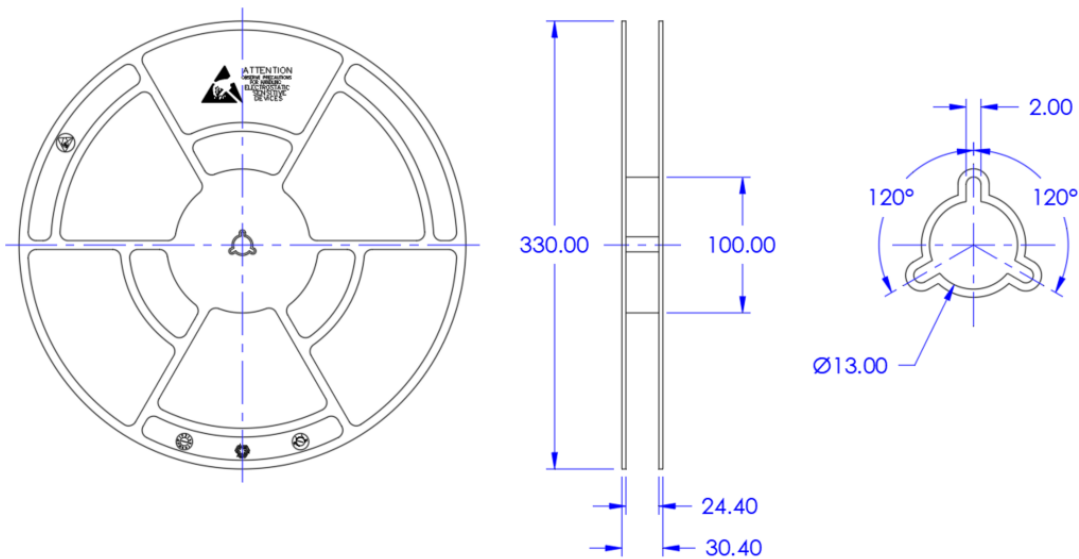


UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
D2PAK (24 mm)	10.80 ±0.10	16.30 ±0.10	4.70 ±0.10	1.50 ±0.10	1.50 +0.1 -0	24.00 ±0.30	1.75 ±0.10	11.50 ±0.10	16.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.35 ±0.10

Exterior		size
Spec 1	W1	16.9±0.1
	W2	1.3±0.1
	W3	1.0±0.1
Spec 2	W1	17.2±0.1 (a)
	W2	1.8±0.1 (b)
	W3	0.85±0.1 (c)

Reel



All dimensions in millimeters
Anti-Static Tape and Reel (T&R)
Quantity per Reel: 800 units



DISCLAIMER

The information contained herein is believed to be reliable; however, Qorvo makes no warranties regarding the information contained herein and assumes no responsibility or liability whatsoever for the use of the information contained herein. All information contained herein is subject to change without notice. Customers should obtain and verify the latest relevant information before placing orders for Qorvo products. The information contained herein, or any use of such information does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other intellectual property rights, whether with regards to such information itself or anything described by such information. THIS INFORMATION DOES NOT CONSTITUTE A WARRANTY WITH RESPECT TO THE PRODUCTS DESCRIBED HEREIN, AND QORVO HEREBY DISCLAIMS ANY AND ALL WARRANTIES WITH RESPECT TO SUCH PRODUCTS WHETHER EXPRESS OR IMPLIED BY LAW, COURSE OF DEALING, COURSE OF PERFORMANCE, USAGE OF TRADE OR OTHERWISE, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Without limiting the generality of the foregoing, Qorvo products are not warranted or authorized for use as critical components in medical, lifesaving, or life-sustaining applications, or other applications where a failure would reasonably be expected to cause severe personal injury or death.

REVISION HISTORY

Revision	Create Date (mm/dd/yyyy)	Description of Change	Initiator of Change
C	11/06/2023	Updated to Qorvo template Updated Package outline drawing based latest drawing revision	Glenn Galang
D	05/21/2024	Added illustration of device orientation on carrier tape (page 3)	Glenn Galang

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

