High Voltage Drivers Technical & Design Overview

ASG/MCC/PCS – Sept, 2022

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Introduction

- This presentation covers several technical aspects of High Voltage Gate Drivers to provide explanations and guidance’s to engineers designing with onsemi devices.

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Agenda

- What is a HVIC driver
- Key Parameters of HVIC drivers
- Design & Components Selection
- Common issues when using HVIC drivers
- PCB Layout Considerations
- Noise Immunity Performance
- Power Losses & Thermal considerations
- Tools and Generic Help

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What is a HVIC driver

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Why using High voltage Gate drivers

- Can be directly connected to a microcontroller
- High current output drive
  - Enable high current driving w/o external current buffer in IGBT & MOSFET application
    (If driving switches in parallel external buffer would be recommended)
- Does not required secondary power supply as power supply is created by bootstrap method
- High dV/dt immunity up to 50V/ns
- Embedded Functions & Protections
  - Under Voltage Lockout (UVLO)
  - Dead-time Control
  - Shut-down Function
  - Current Sensing
  - Thermal Shut-down
  - Fault Output

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Key Specification of High Voltage Gate Drivers

- 3.3 V and 5 V Input Logic Compatible
- Offset Supply Voltage Level (80 V, 200 V, 600 V and 1200 V)
- Driving Current Capability (From 90 mA up to 4.5 A)
- Dynamic Characteristics
  - Turn-On/Off propagation Delay Time
  - Delay matching between Turn-on and off propagation
  - Delay matching between high side and low side (As low as 10ns, 50ns Typ)
  - Turn-on rise time and Turn-off fall time
- Ruggedness
  - CMOS Schmitt-triggered inputs with pull-down for noise immunity
  - dVs/dt transient immunity voltage level (50 V/ns)
  - Allowable negative Vs for high side signal propagation
  - Noise immunity on the supply (Positive and negative)
- Functions
  - Over current protection, Fault reporting, Soft off, built in Bootstrap diode, internal osillator
  - Under Voltage Lockout (UVLO)
  - Dead-time control
  - Shut-down function

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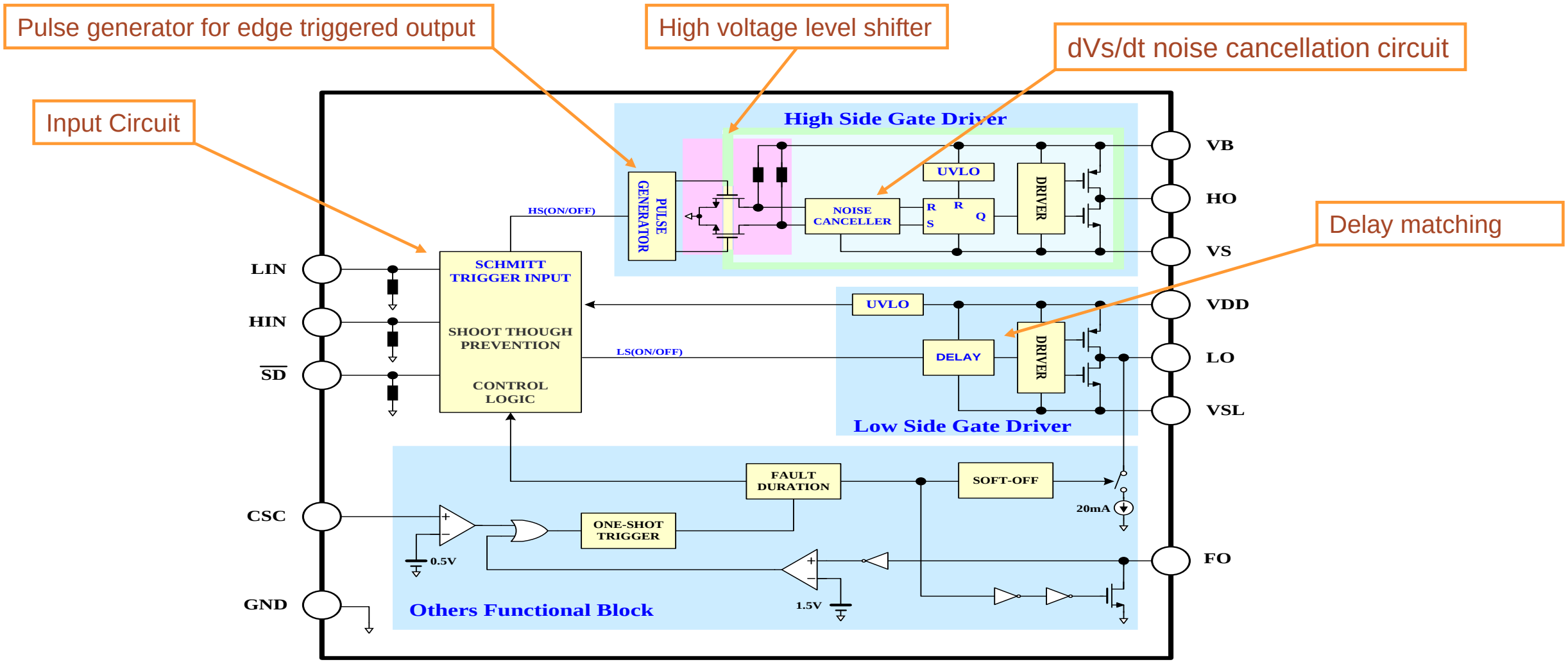
Functional Block Diagram of HV Gate Drive IC



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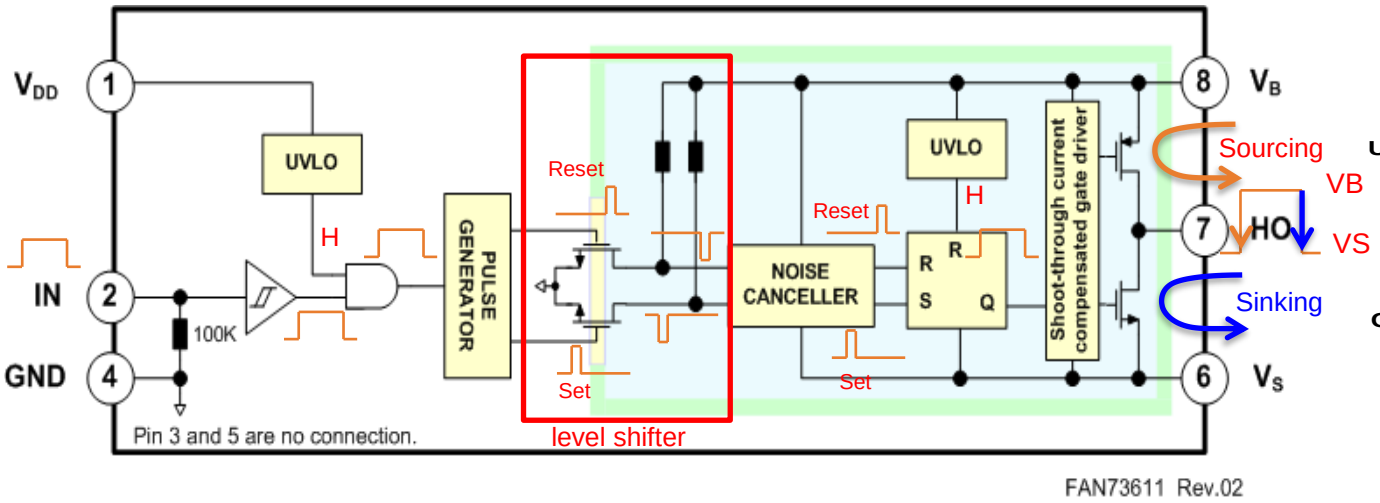
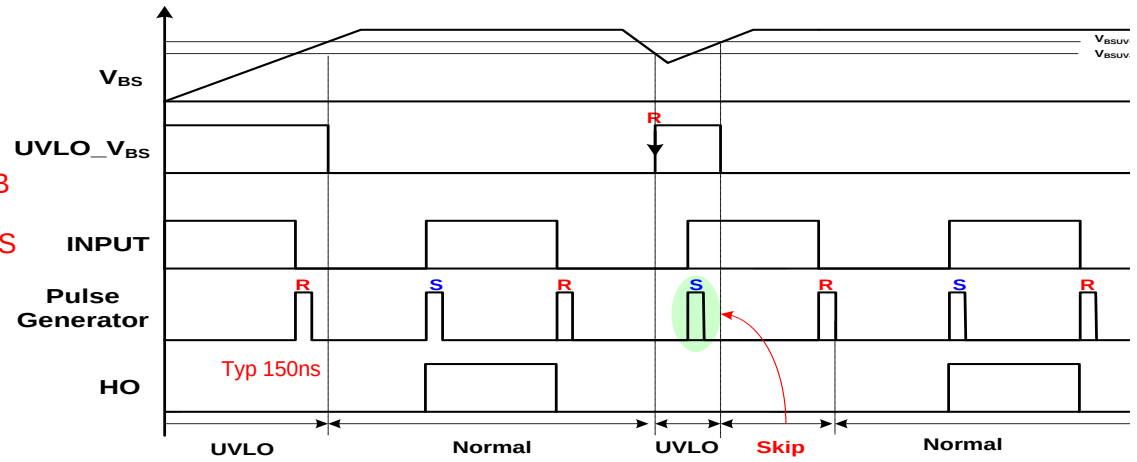
HV Gate Drive IC (HVIC)

Functional Block Diagram



FAN73611 Rev.02

Timing Chart



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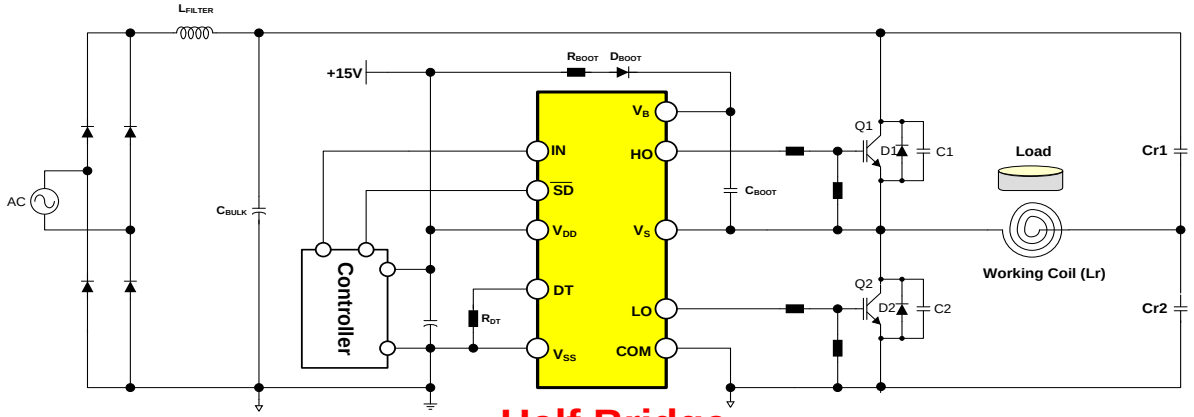
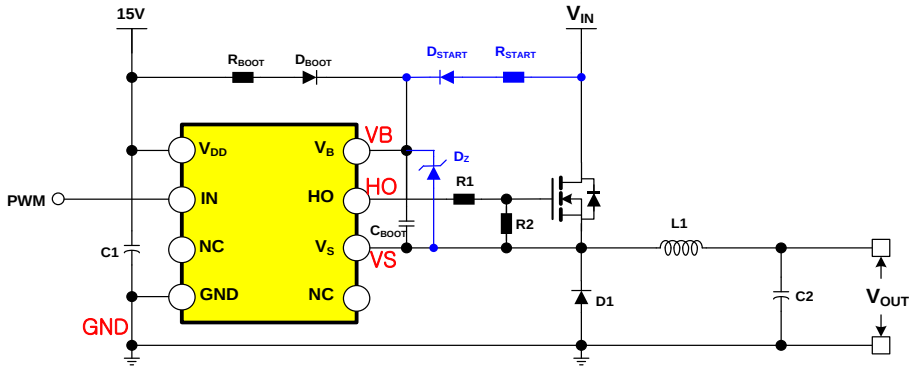
HVIC Main Features

Typical Application Circuit



Half Bridge

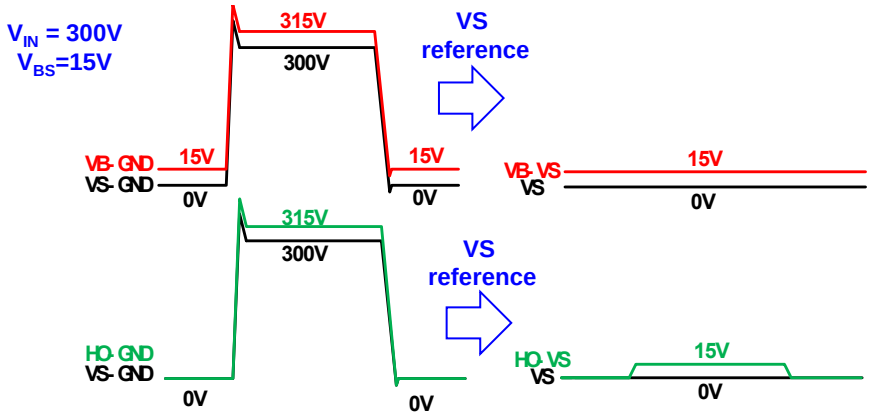


High side Only

Benefits

- ✓ Better noise immunity (due to noise canceling circuit over high dv/dt common-mode noise)
- ✓ Low power consumption (IQBS / IQCC are lower than competitor's device)
- ✓ dVs/dt transient immunity voltage level (50V/ns)
- ✓ Extended allowable negative Vs swing to -9.8V for signal propagation @ VCC=VBS=15V
- ✓ Matched propagation delay below 50nS
- ✓ UVLO functions
- ✓ TTL compatible input threshold levels

Waveform (High side Only)



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Key Parameters of HVIC drivers

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Gate Driver: Key attributes & Requirements

Turn ON/OFF power switch	• Source/Sink Drive strength • Miller Clamp • External VEE input • Split output pins for source / sink	**Choosing drive strength is often a balance between reducing power losses and minimizing EMI**
Level shifting	• Noise Immunity • Separate power and signal ground • Galvanic Isolation	**Negative voltage spikes result from parasitic inductances**
Timing	• Propagation Delay • Delay Matching • Blanking, filters and time to protect	**MOSFETs, used for higher switching frequencies, need shorter propagation delay**
Protection Functions	• Under/Over Voltage Lockout • Shoot Through Prevention • Desat Protection • Overcurrent Protection	Robust gate drive protection features, make the drivers well-suited for all power devices

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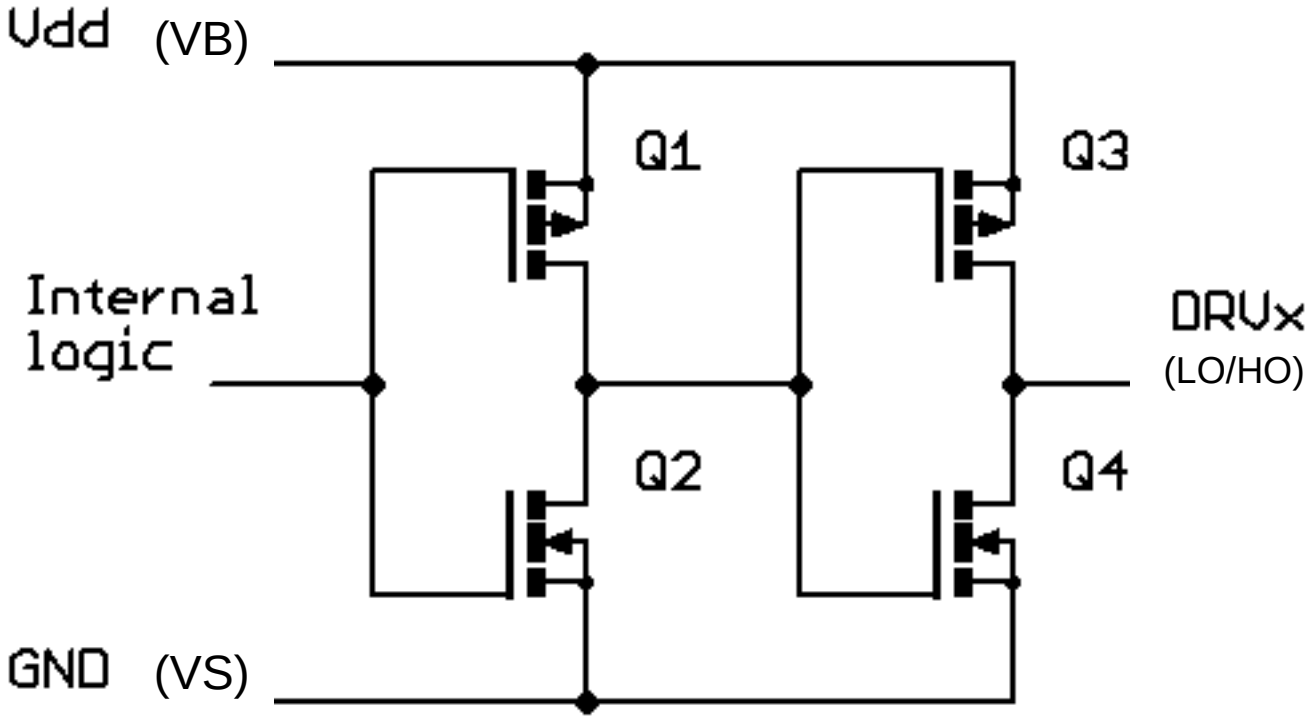
Key parameters of the drivers – Drive peak current



- This is very simplified schematic of the output of the driver. The Q3 and Q4 are the switchers which provides sink and source current described by DS. The Q1 and Q2 has to charge the gate capacitances of Q3 and Q4, this capacitance is higher with larger transistors. The result is, even for zero load capacitance on DRVx pin the rise and fall time will not be zero.
- **Do not just compare the current capability, compare also the rise and fall time for given capacitance.**

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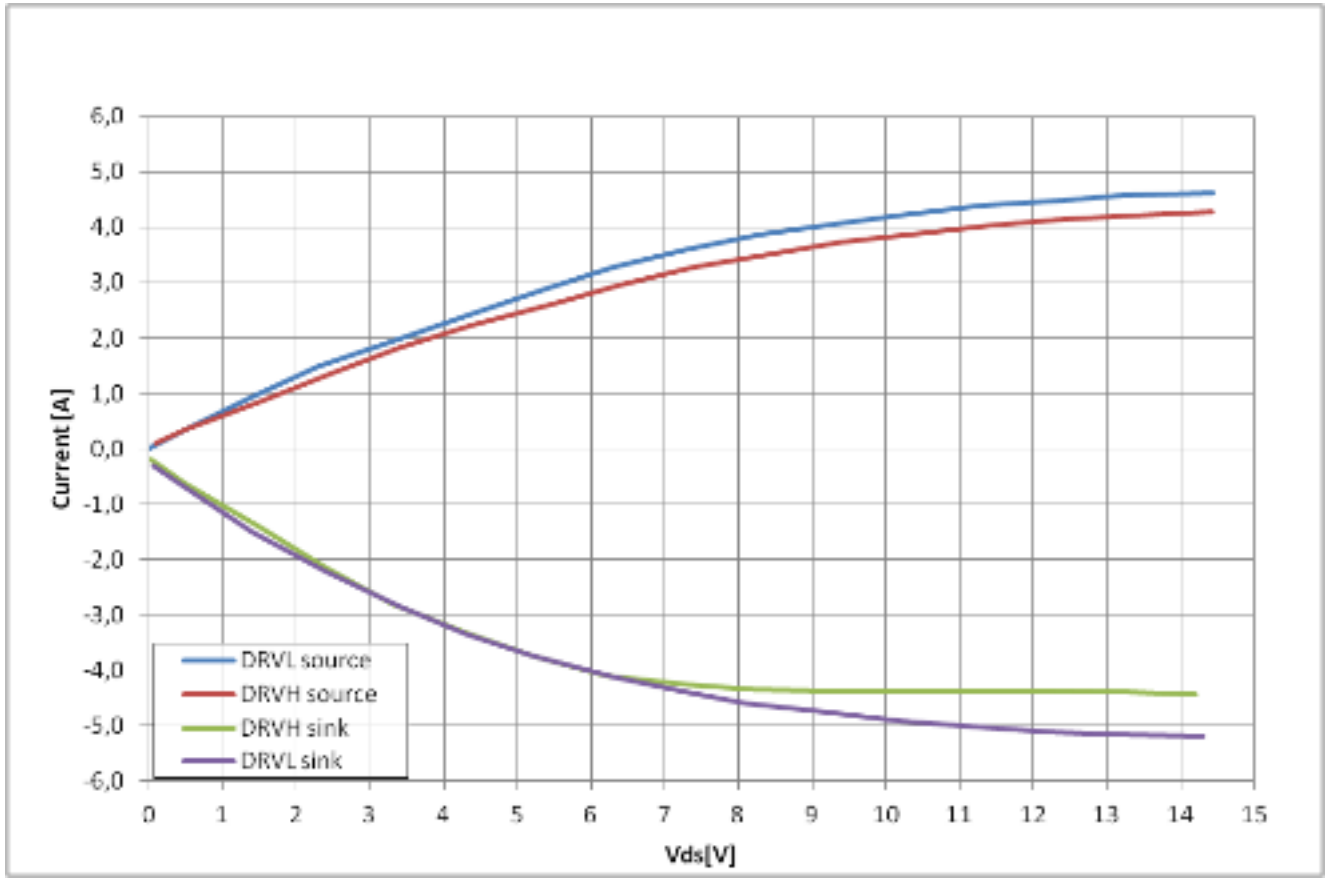
Key parameters of the drivers – Drive peak current



- I_{DRVx_source}, I_{DRVx_sink} – the current value is measured by shorting the DRVx pin to GND or VDD. The value is not stable (here NCP5183). The rise and fall time for given load (capacitor) can be calculated only in case, the current is constant and the current is provided in zero time after turn on/off.
- This is not true, so the stronger driver does not always mean faster turn on/off of the switch !!!
- **Real performance comes from the technology and circuit design.**

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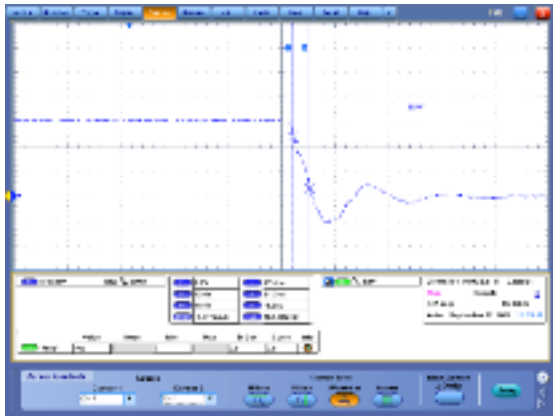
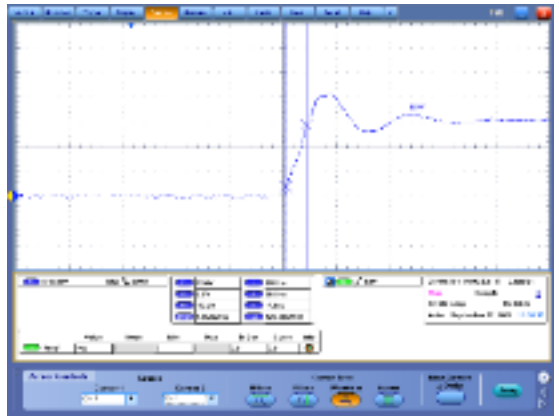
Key parameters of the drivers – Rise/fall time vs. drive current

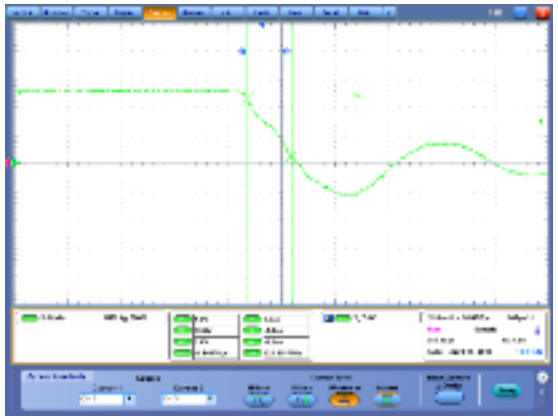


ON – 6 ns

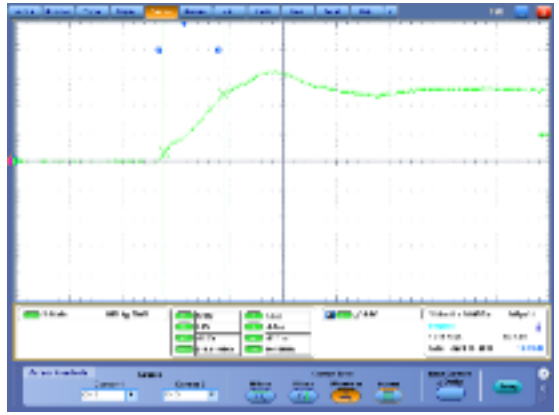


ON – 7 ns

Load – 1nF @ Vcc – 12 V



Compet – 8 ns



Compet – 11 ns

- ON is spec'd as 3.5/3.0 A
- Compet is spec'd as 4.0/4.0A

Peak current capabilities relates to shorter R/F times only at high Cload (>= 10 nF)

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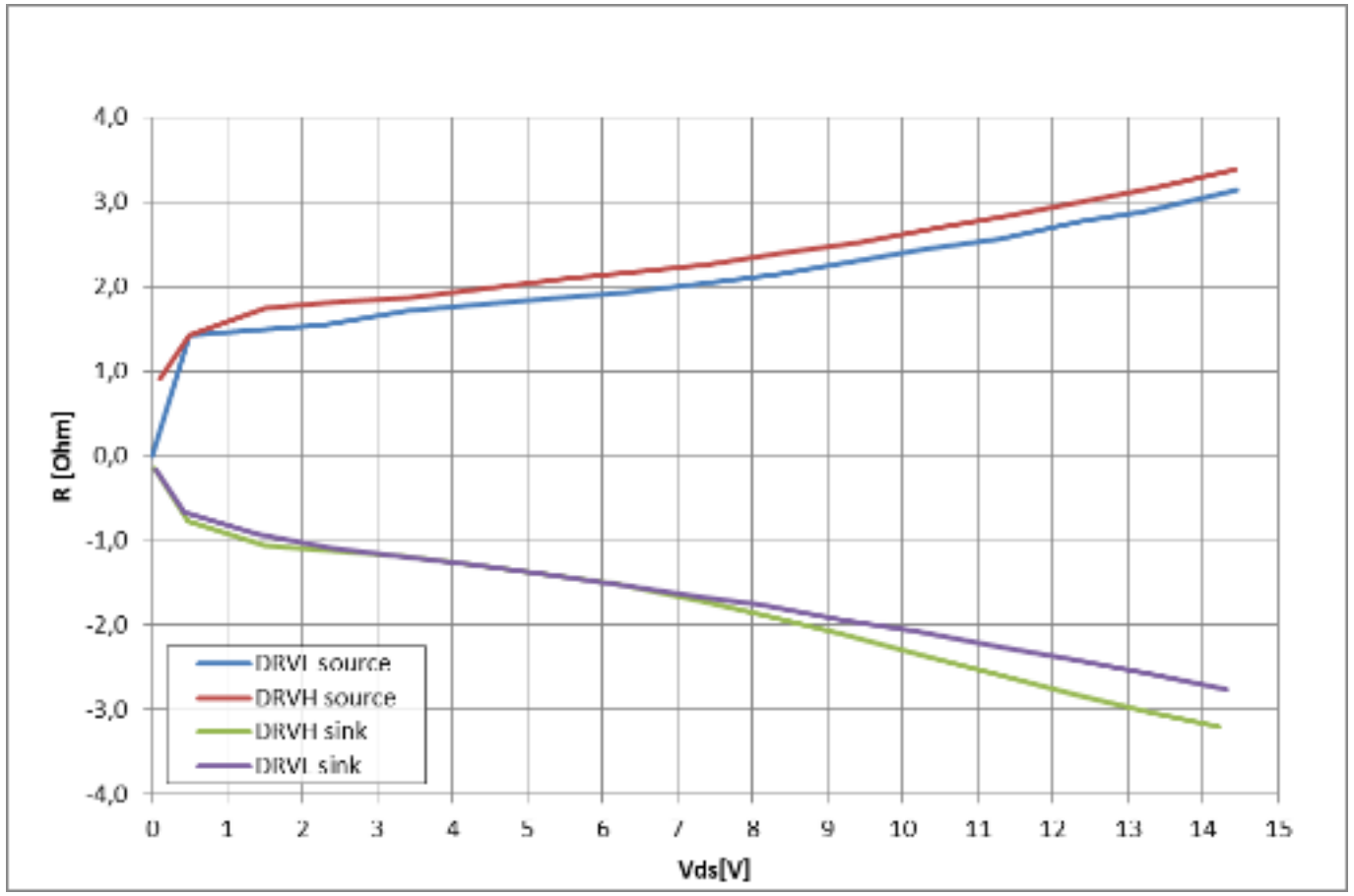
Key parameters of the drivers – Output resistance



- R_{OH}, R_{OL} – the internal resistance of the driver. The parameter is important in case, you want to split power loss between a driver and external gate resistance.
- This Rdson varies with V_{DS}.

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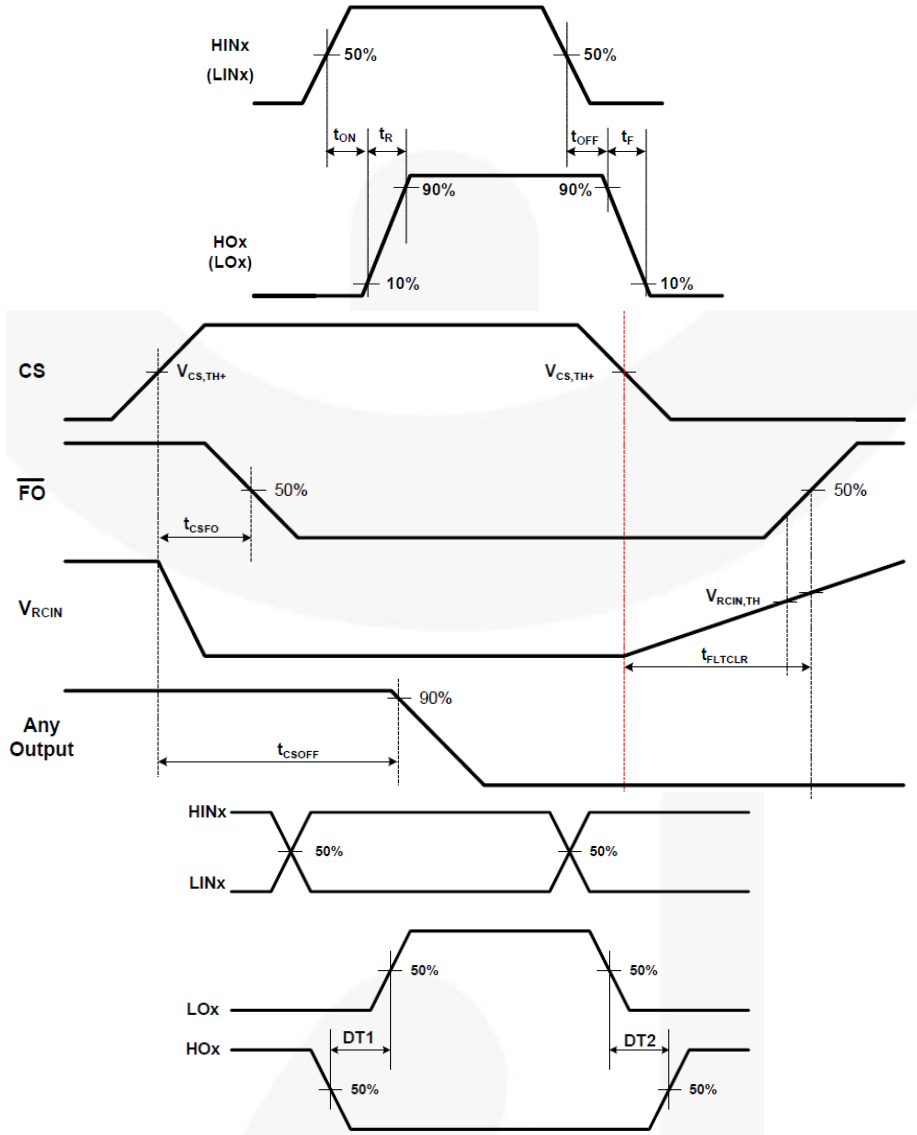
Definition for Dynamic Characteristics

Dynamic Electrical Characteristics

T_A=25°C, V_{BIAS} (V_{DD}, $V_{BS1,2,3}$) = 15.0 V, $V_{S1,2,3}$ = COM, C_{RCIN}=2 nF, and C_{Load} = 1000 pF unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{ON}	Turn-On Propagation Delay	$V_{LIN1,2,3}$=$V_{HIN1,2,3}$=5 V, $V_{S1,2,3}$=0 V	350	500	650	ns
t_{OFF}	Turn-Off Propagation Delay	$V_{LIN1,2,3}$=$V_{HIN1,2,3}$=0 V, $V_{S1,2,3}$=0 V	350	500	650	ns
t_R	Turn-On Rise Time	$V_{LIN1,2,3}$=$V_{HIN1,2,3}$=5 V	20	50	100	ns
t_F	Turn-Off Fall Time	$V_{LIN1,2,3}$=$V_{HIN1,2,3}$=0 V	10	30	80	ns
t_{EN}	Enable LOW to Output Shutdown Delay		400	500	600	ns
t_{CSBLT}	CS Pin Leading-Edge Blanking Time		400	650	850	ns
t_{CSFO}	Time from CS Triggering to $\overline{FO}$	From V_{CSC}=1 V to $\overline{FO}$ Turn-Off		850	1300	ns
t_{CSOFF}	Time from CS Triggering to Low-Side Gate Outputs Turn-Off	From V_{CSC}=1 V to Starting Gate Turn-Off		850	1300	ns
t_{FLTIN}	Input Filtering Time(6) (HINx, LINx, EN)		170	250	330	ns
t_{FLTCLR}	Fault-Clear Time			1.30	2.35	ms
* DT	Dead Time		230	320	400	ns
MDT	Dead-Time Matching (All Six Channels)(7)	| DT1−DT2 |			50	ns
* MT	Delay Matching (All Six Channels)(8)				50	ns
PM	Output Pulse-Width Matching(9)	PW_{IN} > 1 µs PW_{IN} −PW_{OUT}		50	100	ns

*DT1 : Dead Time @ HO Turn−off to HO Turn−on
*DT2 : Dead Time @ LO Turn−off to LO Turn−on
* MTON: Delay Matching, HO & LO Turn−on
* MTOFF: Delay Matching, HO & LO Turn−off



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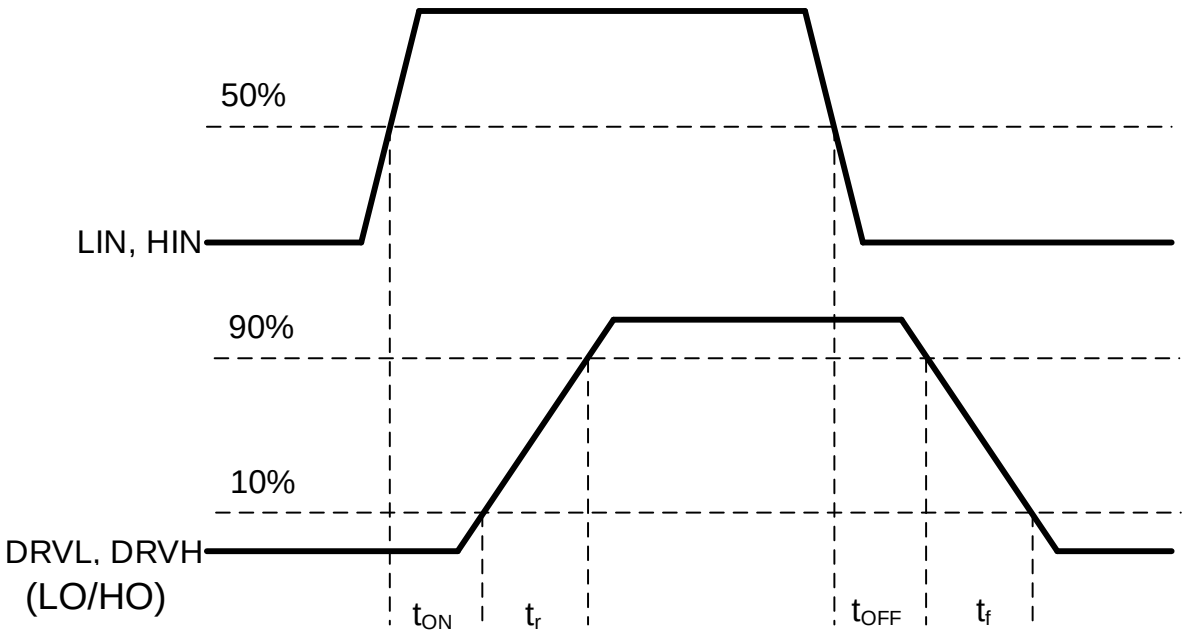
Key parameters of the drivers - Prop delays & Rise/Fall Times



t_{ON}, t_{OFF} – is the time needed for pulse to pass through the device. Input signal sharp edge, output one measured at 10%, to measure just **propagation delay**, not driver capability. When there is an input filter, the filter time is included into the propagation delay

t_r, t_f – is the time needed to charge and discharge a capacitor of specific value (usually 1 nF). The **rise and fall time** are somehow linked with driver current capability but not directly.

Higher driver current does not directly translate into shorter Turn-On/Turn-Off times.

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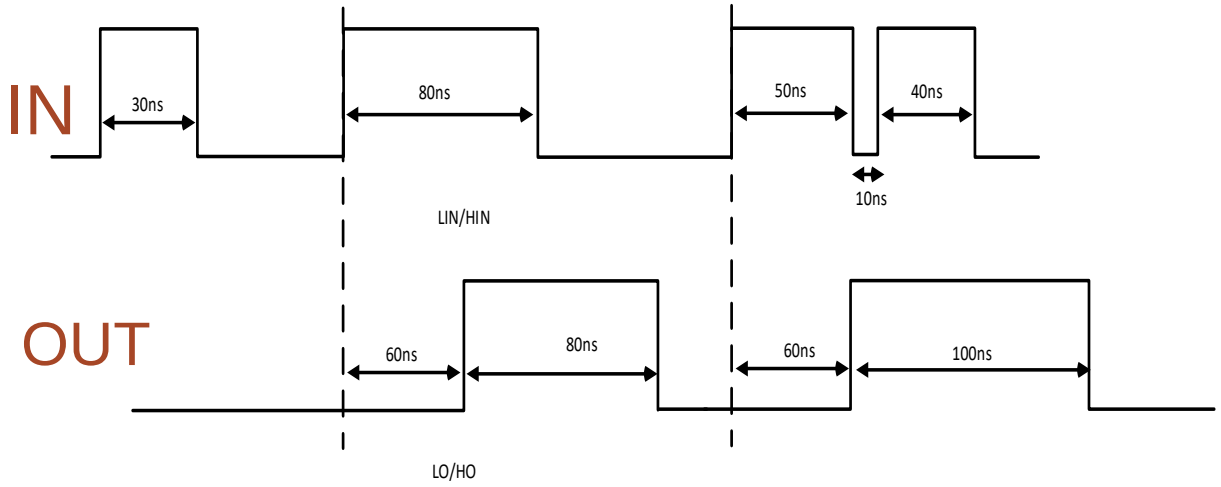
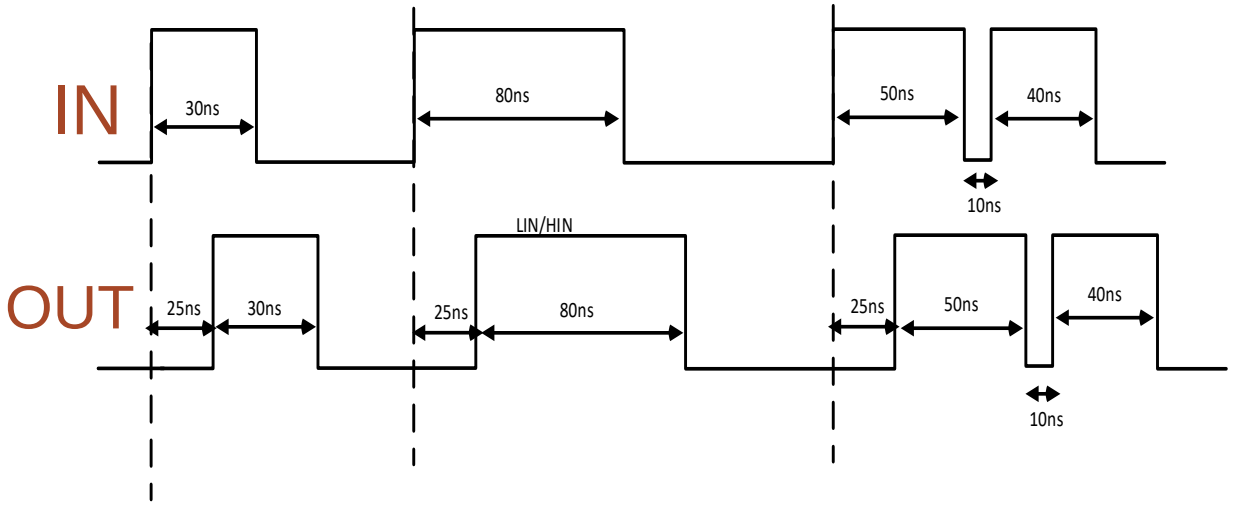
Key parameters of the drivers - Input Filters & Impact on Prop. delay

Input filter function is demonstrated on NCP51530 device. Versions A and B are available:
The A version, features a noise rejection function to ensure that any pulse glitch shorter than 30 ns will not produce any output change.
The B version, has no such filters in the input stages, the output signal is just delayed.



NCP51530A (Input Filter)



NCP51530B

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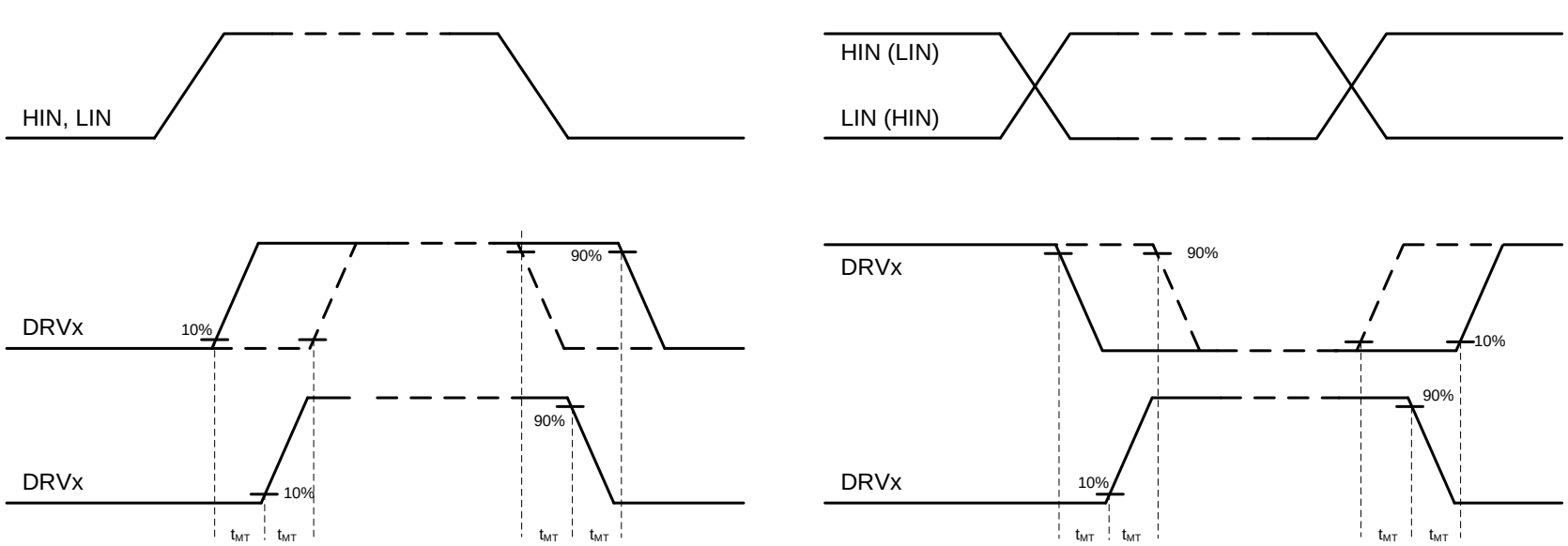
Key parameters of the drivers – Delay Matching



- t_{MT} – delay matching time. During testing four values are measured. The propagation delay for low side and high side driver, for positive and negative pulses.
- It is the time difference between the output of both channels

- **When paralleling When paralleling MOS they're driven simultaneously**
- **Gate drivers outputs to increase driving capabilities**

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Conditions for Safe Operation

Absolute Maximum Ratings

Symbol	Characteristics	Min.	Max.	Unit
V_S	High-side offset voltage	V_B-25	V_B+0.3	V
V_B	High-side floating supply voltage	-0.3	625	
V_{HO}	High-side floating output voltage HO	V_S-0.3	V_B+0.3	
V_{CC}	Low-side and logic fixed supply voltage	-0.3	25	
V_{LO}	Low-side output voltage LO	-0.3	V_{CC}+0.3	
V_{IN}	Logic input voltage (HIN, LIN)	-0.3	V_{CC}+0.3	
COM	Logic ground	V_{CC}-25	V_{CC}+0.3	
dV_S/dt	Allowable offset voltage slew rate		50	V/ns
P_D(2)(3)(4)	Power dissipation	8-SOP	0.625	W
		14-SOP	1.0	
		8-DIP	1.2	
θ_{JA}	Thermal resistance, junction-to-ambient	8-SOP	200	°C/W
		14-SOP	110	
		8-DIP	100	
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature		150	°C

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Risk Factors of Malfunction

Factors related to Process

Symbol	Characteristics	Min.	Max.	Unit
V_S	High-side offset voltage	V_B-25	V_B+0.3	V
V_B	High-side floating supply voltage	-0.3	625	
V_{HO}	High-side floating output voltage HO	V_S-0.3	V_B+0.3	
V_{CC}	Low-side and logic fixed supply voltage	-0.3	25	
V_{LO}	Low-side output voltage LO	-0.3	V_{CC}+0.3	
V_{IN}	Logic input voltage (HIN, LIN)	-0.3	V_{CC}+0.3	

Basic Characteristics

V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply under-voltage positive going threshold		8.2	9.2	10.0	V
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply under-voltage negative going threshold		7.6	8.7	9.6	
V_{CCUVH} V_{BSUVH}	V_{CC} supply under-voltage lockout hysteresis			0.6		
V_{IH}	Logic "1" input voltage		2.9			V
V_{IL}	Logic "0" input voltage				0.8	
V_S	Allowable negative V_S pin voltage for HIN signal propagation to HO			-9.8	-7.0	V

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Design & Components Selection

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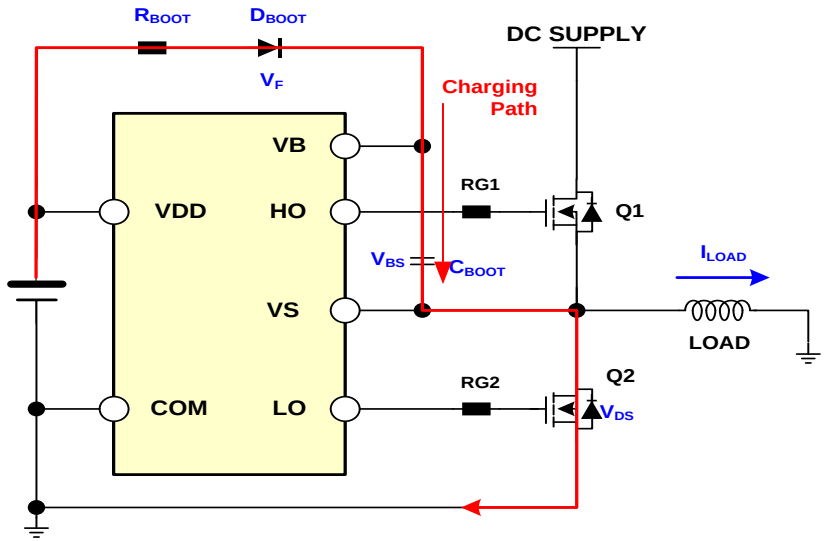
How to select the Bootstrap Capacitor (1/2)



A resistor (R_{BOOT}) is placed in series with bootstrap diode so to limit the current when the bootstrap capacitor is initially charged. The value should not exceed the ohms (typically 5~10 Ω), which would increase the VBS time constant .

Time Constant $\tau = \frac{R_{BOOT} \cdot C_{BOOT}}{D}[s]$ (≒ 3nC)

Minimum Value of CBOOT

$$C_{BOOT\,min} = \frac{Q_{TOTAL}}{\Delta V_{BOOT}}$$

Total charge of the bootstrap capacitor

$$Q_{TOTAL} = Q_{GATE} + (I_{LKCAP} + I_{LKGS} + I_{QBS} + I_{LK} + I_{LKDIODE}) \times t_{ON} + Q_{LS}$$

Maximum allowable voltage drop on CBOOT

$$\Delta V_{BOOT} = V_{DD} - V_F - V_{GSMIN}$$

Symbol	Description
Q_{GATE}	Total Gate charge
I_{LKCAP}	Bootstrap capacitor leakage current
I_{LKGS}	Switch gate-source leakage current
I_{QBS}	Bootstrap circuit quiescent current
I_{LK}	Bootstrap circuit leakage current
I_{LK_DIODE}	Bootstrap diode leakage current
T_{ON}	High side on time
Q_{LS}	Charge required by the internal level shifters

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How to select the Bootstrap Capacitor (2/2)

◆ Design Example (HVIC : FAN7382, Switching Device : FCP20N60, Bootstrap Diode : UF4007)

If the maximum allowable voltage drop on the bootstrap capacitor is 1.0V during the high side switch on state, the minimum capacitor value is calculated by the as following equation

$$Q_{TOTAL} = Q_{GATE} + (I_{LKCAP} + I_{LKGS} + I_{QBS} + I_{LK} + I_{LKDIODE}) \cdot T_{ON} + Q_{LS}$$

$$Q_{TOTAL} = (98\times10^{-9}) + \{(100\times10^{-9} + 120\times10^{-6} + 50\times10^{-6} + 10\times10^{-9})\} \times (25\times10^{-6}) + (3\times10^{-9}) = 105.2\times10^{-9}[C]$$

$$C_{BOOT} = \frac{Q_{TOTAL}}{\Delta V_{BOOT}} = \frac{105.2\times10^{-9}}{1} \cong 105[nF]$$

The voltage drop due to the external diode is nearly 0.7V. We have assumed the capacitor charging time equal to the high side on time (duty cycle 50%)
Where as different bootstrap capacitor, The Voltage drop is

- 100 nF → $\Delta V_{BOOT} = \frac{Q_{TOTAL}}{C_{BOOT}} = \frac{105nC}{100nF} = 1.05[V]$
- 150 nF → $\Delta V_{BOOT} = \frac{Q_{TOTAL}}{C_{BOOT}} = \frac{105nC}{150nF} = 0.7[V]$
- 220 nF → $\Delta V_{BOOT} = \frac{Q_{TOTAL}}{C_{BOOT}} = \frac{105nC}{220nF} = 0.48[V]$
- 570 nF → $\Delta V_{BOOT} = \frac{Q_{TOTAL}}{C_{BOOT}} = \frac{105nC}{570nF} = 0.18[V]$

<Design Input Parameter>

Q_{GATE} =98nC (Maximum)
I_{LKGS} =100nA (Maximum)
I_{LKCAP} =0 (Used ceramic capacitor)
I_{QBS} =120uA (Maximum)
I_{LK} =50uA (Maximum)
Q_{LS} = 3nC
T_{ON} = 25us (Duty=50% @ fs=20KHz)
$I_{LKDIODE}$ = 10nA

Suggested values are within the range of 100nF ~ 570nF, but the right value must be selected according to the application in which the device is used, when the capacitor value is too big, the bootstrap charging time is slowed and the low side on time might be not long enough to reach the right bootstrap voltage

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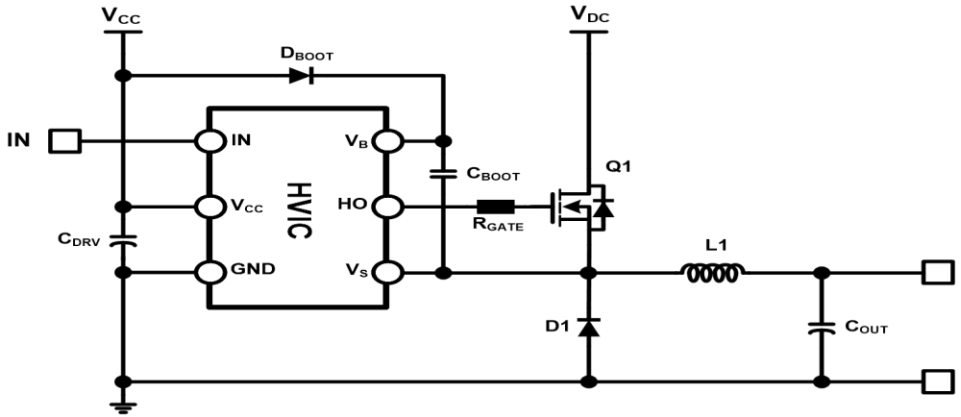
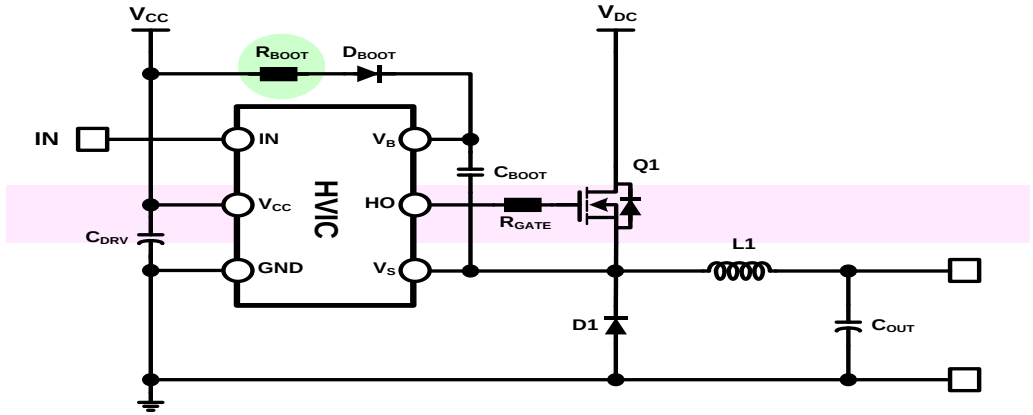
Possible Remedies against Bootstrap Circuit Problem

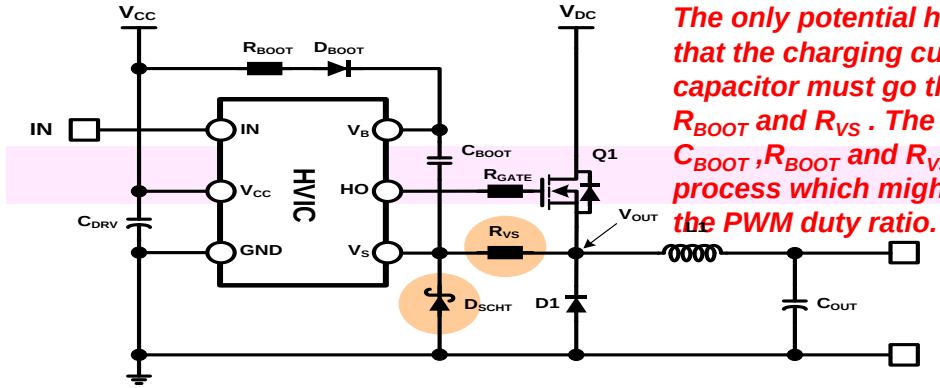
Adding a small resistor (R_{BOOT}) in series with bootstrap diode





This method can mitigate the problem. Unfortunately, the series resistor (R_{BOOT}) does not provide a foolproof solution against an over voltage and it also slows down the recharge process of the bootstrap capacitor.
we suggest the bootstrap resistor, R_{BOOT}, not exceeding some Ohms (Typically 5~10Ohms) to avoid increasing the V_{BS} time constant.

The gate resistor was split into two resistors (R_{GATE} and R_{VS}) and adding a low forward voltage drop schottky diode from ground to V_S.



The only potential hazard by this circuit is that the charging current of the bootstrap capacitor must go through two resistors, R_{BOOT} and R_{VS} . The time constant of C_{BOOT} ,R_{BOOT} and R_{VS} slows the recharge process which might be a limiting factor as the PWM duty ratio.

The gate resistor split into R_{GATE} and R_{VS} has a double purpose:
It sets the turn-on and turn-off speed in the MOSFET and also provide current limiting for the schottky diode during the negative voltage transient of the source terminal of the main switch. In additional, the bootstrap capacitor is protected against over voltage by the two diodes connected to the ends of C_{BOOT}.

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Summary of Bootstrap Components Selection

✓The bootstrap resistor must be considered in sizing the bootstrap resistance that the current developed during initial bootstrap charge. If a resistor is needed in series with the bootstrap diode.

✓The bootstrap capacitor using low-ESR capacitor such as ceramic capacitor.

✓And the capacitor from V_{CC} to COM supports both the low-side driver and bootstrap recharge.
We recommended a value at least 10 times higher than bootstrap capacitor

✓The bootstrap diode must be used a lower forward voltage drop and switching time as soon as possible fast recovery such as ultra-fast.

You can see more detailed information.
Please refer to application note, **AND-9674 :** Design and Application Guide of Bootstrap Circuit for HV Gate Driver IC

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How to dimension the gate resistance (1/2)

◆ Gate Resistances

The switching speed of the output transistor (MOSFET or IGBT) can be adjusted sizing the turn-on/off resistors controlling the turn-on and turn-off gate current.

✓ Sizing the turn-on gate resistor

Gate resistance may be chosen in order to fix either the switching-time or the output voltage slope.
To obtain the desired switching time the gate resistance can be sized starting from Qgs, Qgd, VDD (or VBS), and Vgs.

$$I_{g(avr)} = \frac{Q_{gs} + Q_{gd}}{t_{SW}} \qquad R_{g(ON)} = R_{Total} - R_{DRV(ON)} = \frac{V_{DD} - V_{gs(th)}}{I_{g(avr)}} - \frac{V_{DD}}{I_{Source}}$$

Where, $R_{g(ON)}$ is the gate on resistance and $R_{DRV(ON)}$ is the driver equivalent on resistance.

✓ Output voltage slope and relation with turn-on resistor

Turn-on resistor can be sized to control output voltage slope. (dVout/dt)

$$\frac{dV_{out}}{dt} = \frac{I_{g(avr)}}{C_{gd(off)}} \qquad \text{Therefore,} \quad R_{Total} = \frac{V_{DD} - V_{gs(th)}}{I_{g(avr)}} = \frac{V_{DD} - V_{gs(th)}}{C_{gd(off)} \frac{dV_{out}}{dt}}$$

Where, $C_{gd(off)}$ is the Miller effect capacitor, specified as C_{rss} in the datasheet.

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How to dimension the gate resistance (2/2)

✓ Sizing the turn-off gate resistor

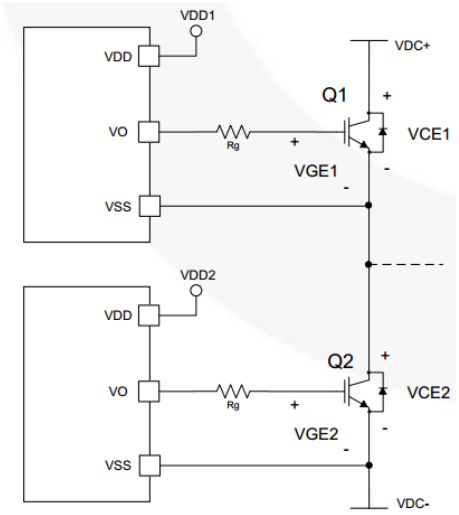
Turn-off gate resistor must be sized with applying worse case that the drain of the MOSFET in turn-off state is forced to commutate by external events.

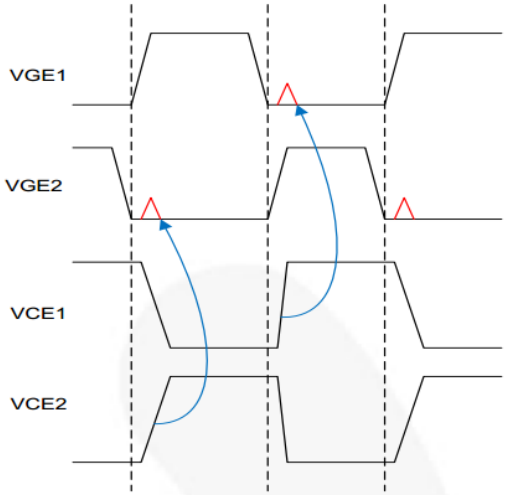
The following equation relates the MOSFET gate threshold voltage to the drain dv/dt;

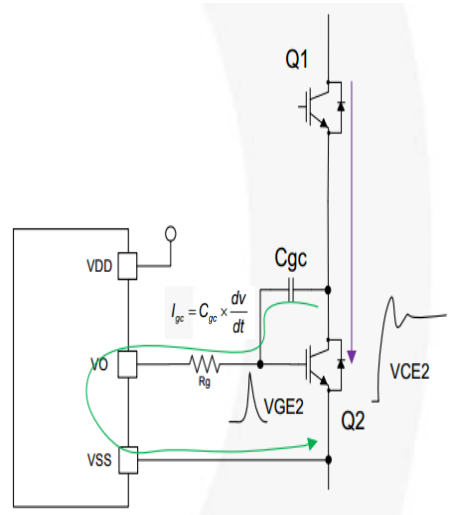
$$V_{gs(th)} \geq (R_{g(off)} + R_{DRV(off)}) \cdot I_g = (R_{g(off)} + R_{DRV(off)}) \cdot C_{gd} \frac{dV_{out}}{dt}$$

$$R_{g(off)} \leq \frac{V_{gs(th)}}{C_{gd} \cdot \frac{dV_{out}}{dt}} - \frac{V_{DD}}{I_{Sink}}$$

Where, $R_{g(off)}$ is the gate on resistance, and $R_{DRV(off)}$ is the driver equivalent resistance







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Common issues when using HVIC drivers

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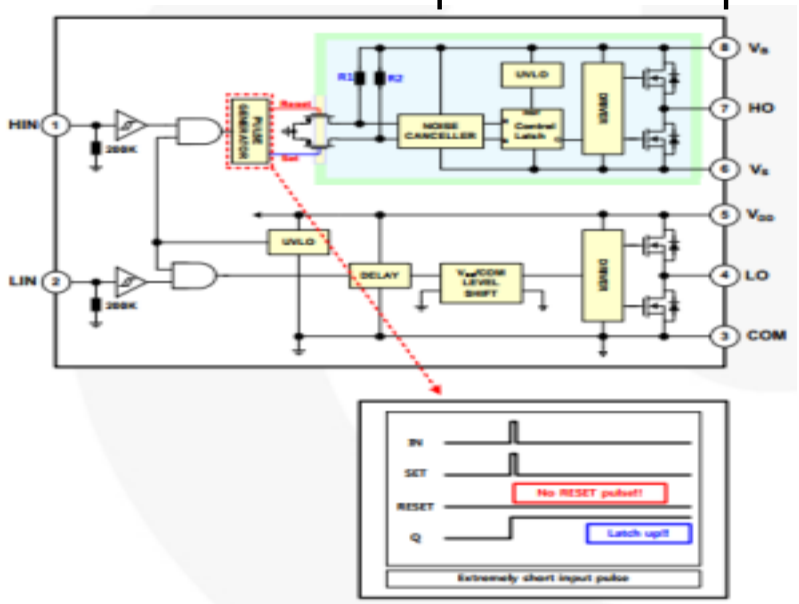
Latch-up Problem for Short Pulse input

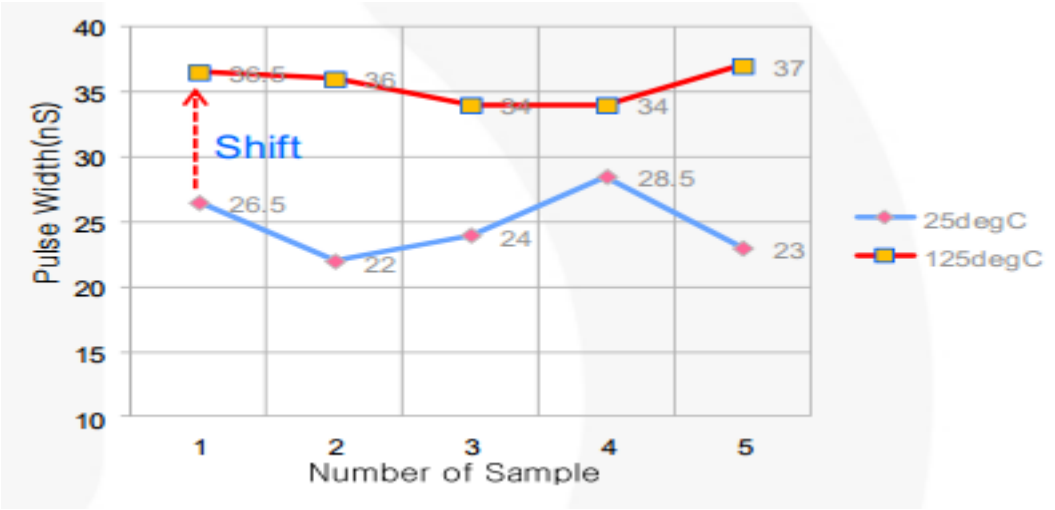
Basically HVIC can transfer about 70 ns pulse, even though input Pulse Width is shorter than internal Pulse Width(typ. 150 ns) of short pulse generator.
But, It is necessary to protect against narrow PWM pulses lower than 100 ns. Generally, recommended min input pulse is 100 ns to avoid response or any malfunction of HVIC.
Please refer to AN-8102 : Recommendations to Avoid Short Pulse Width Issues in HVIC Gate Driver Applications

Latest generations of HV drivers can work with shorter Input signals

<Root-cause of Short pulse latch-up >



<Test Result; Pulse width of Latch-up>



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PCB Layout Considerations

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Layout General Guidelines

- **Printed Circuit Board Layout : Gate Driver**

  The "Layout" for minimized stray inductances as follows:

  ✓Direct tracks between switches with no loops or deviation.

  ✓Avoid interconnect links. These can add significant inductance.

  ✓Reduced the effect of lead-inductance by lowering package height above the PCB.

  ✓Consider co-locating both power switches to reduce track length.

  ✓Placement and routing for supply capacitor and gate resistors as close as possible to HVIC.

  ✓The bootstrap diode as close as possible to bootstrap capacitor.

- **Printed Circuit Board Layout : Super Junction MOSFET**

✓ • To achieve the best performance of Super-Junction MOSFETs, optimized layout is
✓ required
✓ • Gate driver and Rg must be placed as close as possible to the MOSFET gate pin
✓ • Separate POWER GND and GATE Driver GND
✓ • Minimize parasitic C_{gd} capacitance and source inductance on PCB
✓ • For paralleling Super-Junction MOSFETs, symmetrical layout is mandatory
✓ • To reduce oscillation, slow down dv/dt and di/dt by increasing Rg or using ferrite bead

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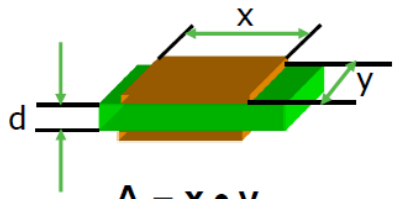
Examples with High External C_{GD} & Reduced C_{GD}

High External C_{GD}

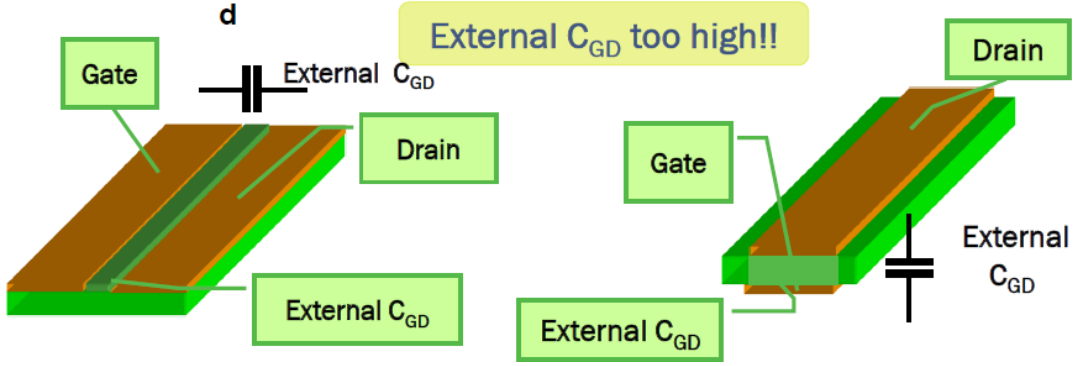


$$A = x \bullet y$$

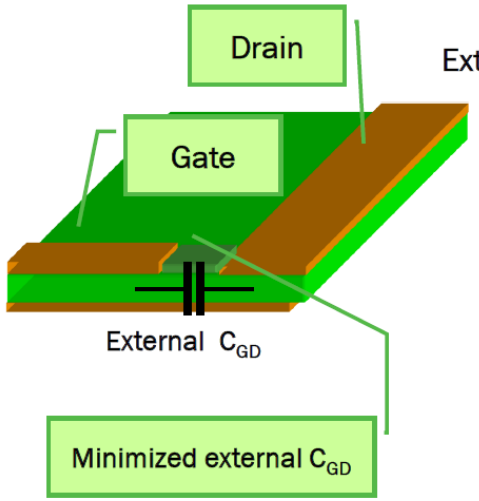
$$C = \frac{\varepsilon_0 \bullet \varepsilon_r \bullet A}{d}$$

Capacity between trace pitches

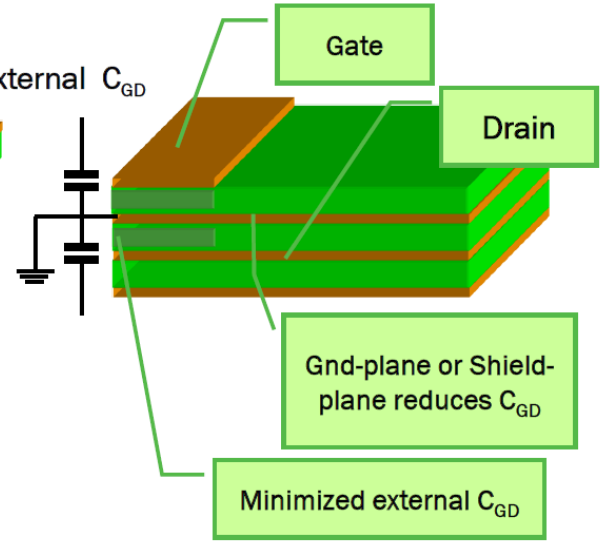
External C_{GD} too high!!



Minimized External C_{GD}



(a) double layer PCB



(b) multi layer PCB

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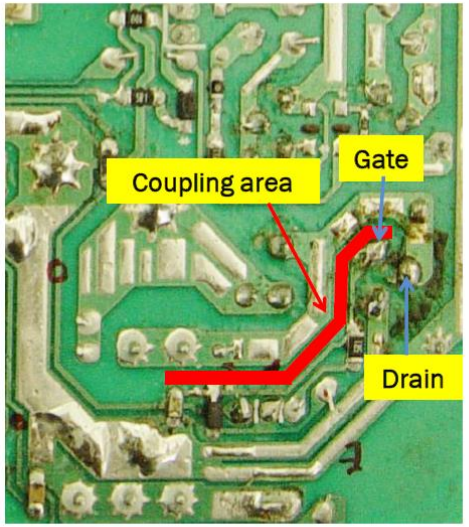
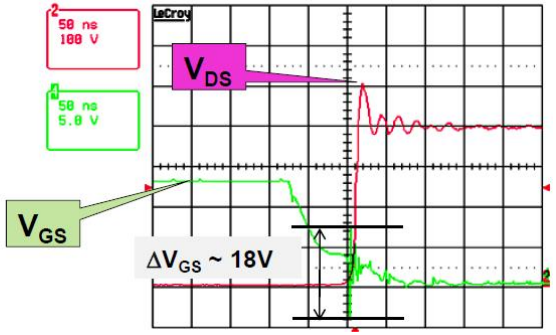
Examples with High External C_{GD} & Reduced C_{GD} – Spikes During Turn off

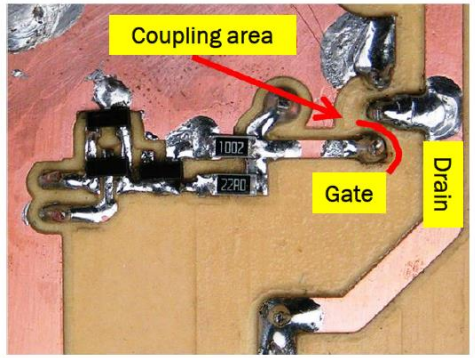
High External C_{GD} – Higher Spikes

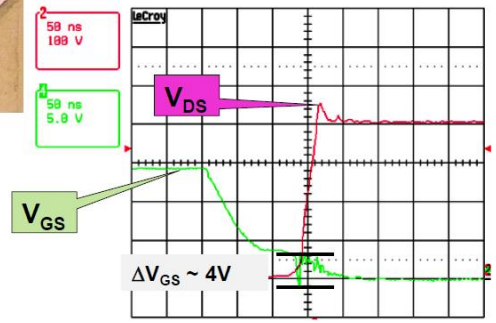
PCB example with high external C_{GD}





Minimized External C_{GD} – Lower Spikes





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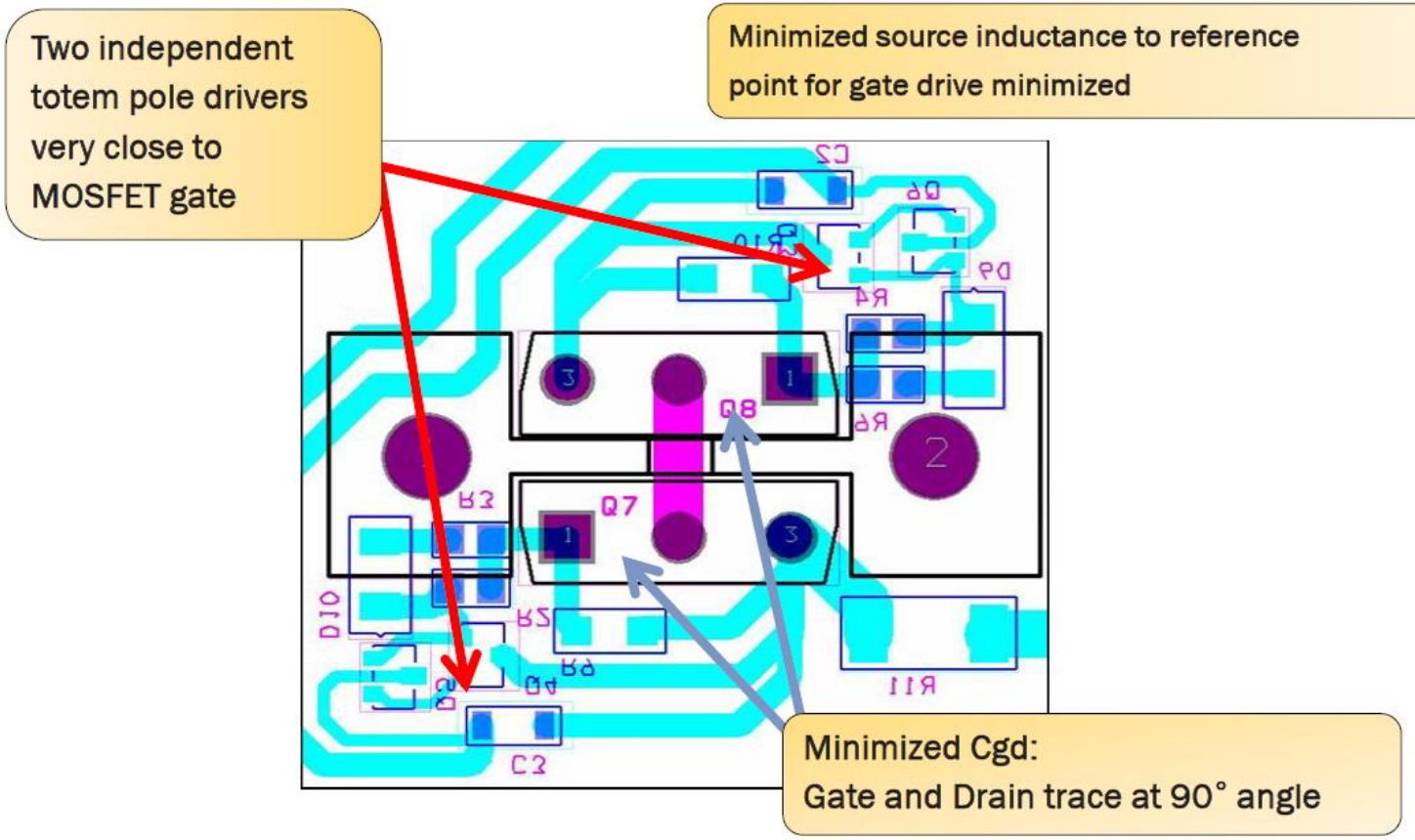
Paralleling MOSFETs



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Noise Immunity Performance

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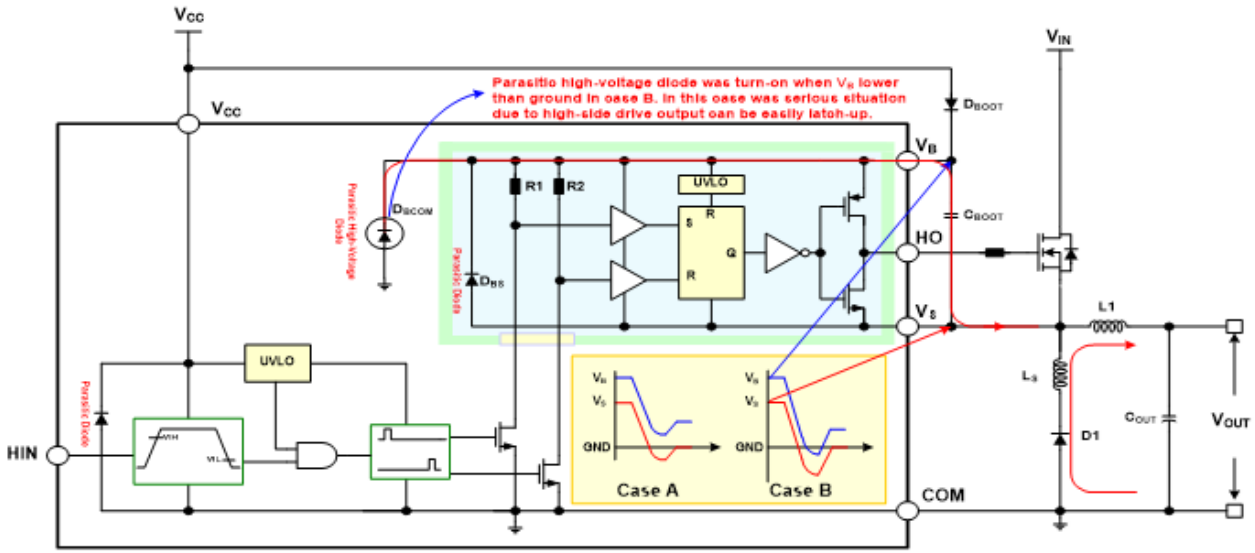
Why undershoot spike can be present on Vs ?

- When there is negative voltage at the source of the switching device during turn-off it causes load current to flow in the low-side freewheeling diode as shown in below Figure. In this case, the inductive stray elements, L_S, may push Vs below COM. The amplitude of negative voltage is proportional to the stray inductances and the turn-off speed, di/dt, of the switching device.



- The amplitude of negative voltage given by as below equation,

$$V_S - COM = -(L_S)\frac{di}{dt}$$

- For example, in a 10 A gate driver with 100 nH stray inductance has a 50 ns switching time, the amplitude of negative voltage spike between Vs and ground is -20 V.

$$V_S - COM = -(100 \times 10^{-9})\frac{10}{50 \times 10^{-9}} = -20[V]$$

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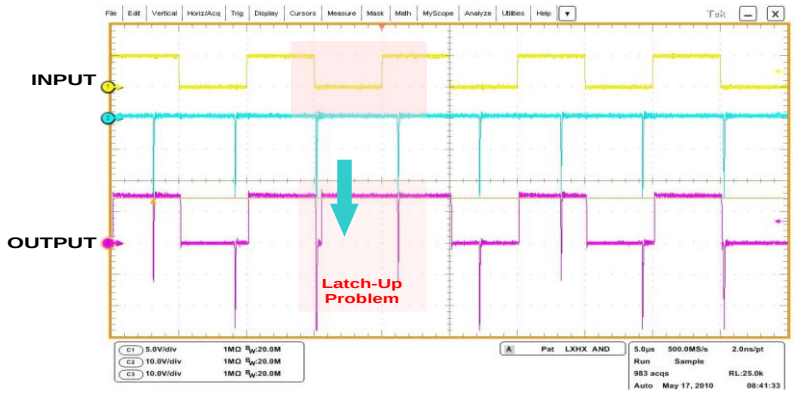
Why is undershoot spike on Vs pin important ?

✓ Effects of the undershoot spike on the output pin (Vs)

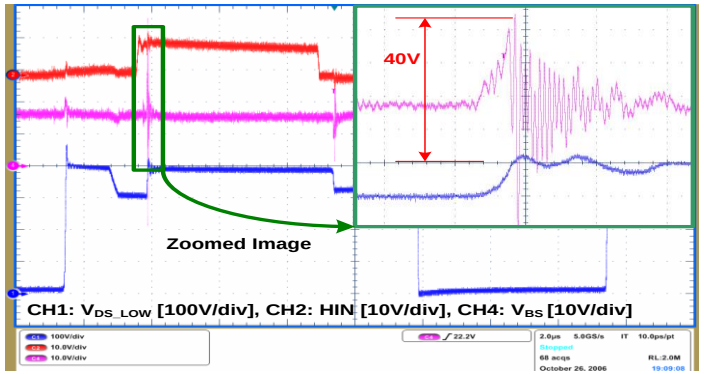
Case 1. If undershoot voltage is present on Vs pin, the high side output will temporarily latch in its current state.
→ Happen when upper and lower switches are short-circuit condition in Half-Bridge topology.

Case 2. If the output pin undershoot spike has a duration in the order to of tenths of nanoseconds the bootstrap capacitor can become overcharged.
→ Exceed the absolute maximum voltage (V_{BS}) limits in the high side gate driver

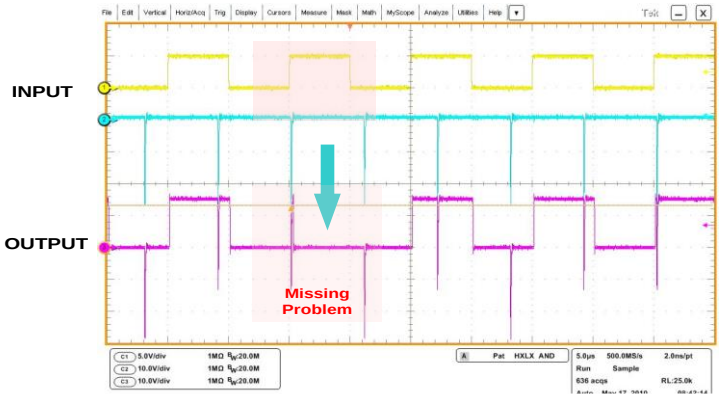
Case 3. Provided Vs remains within absolute maximum limits the IC will not suffer damages, however if Vs is lower than “Allowable negative Vs voltage” which was specified in the data sheet, input signal for high-side cannot be delivered to the high-side gate driver while undershoot
→ At this situation, the level shifter of the HVIC suffers from a lack of the operating voltage headroom.



Case 1



Case 2



Case 3

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The Definition of NPSOA (Neg. Pulse Safety of Area)

- When high side MOSFET is turned off, negative VS undershoot occurs by low side freewheeling current. Excessive negative VS undershoot can result in malfunction or destruction of HVIC

- VS-NPSOA describe allowable negative VS in terms of negative pulse width and voltage level

※ Note : We do not guarantee Recommended SOA regarding MP condition, but just provide reference data according to test results.

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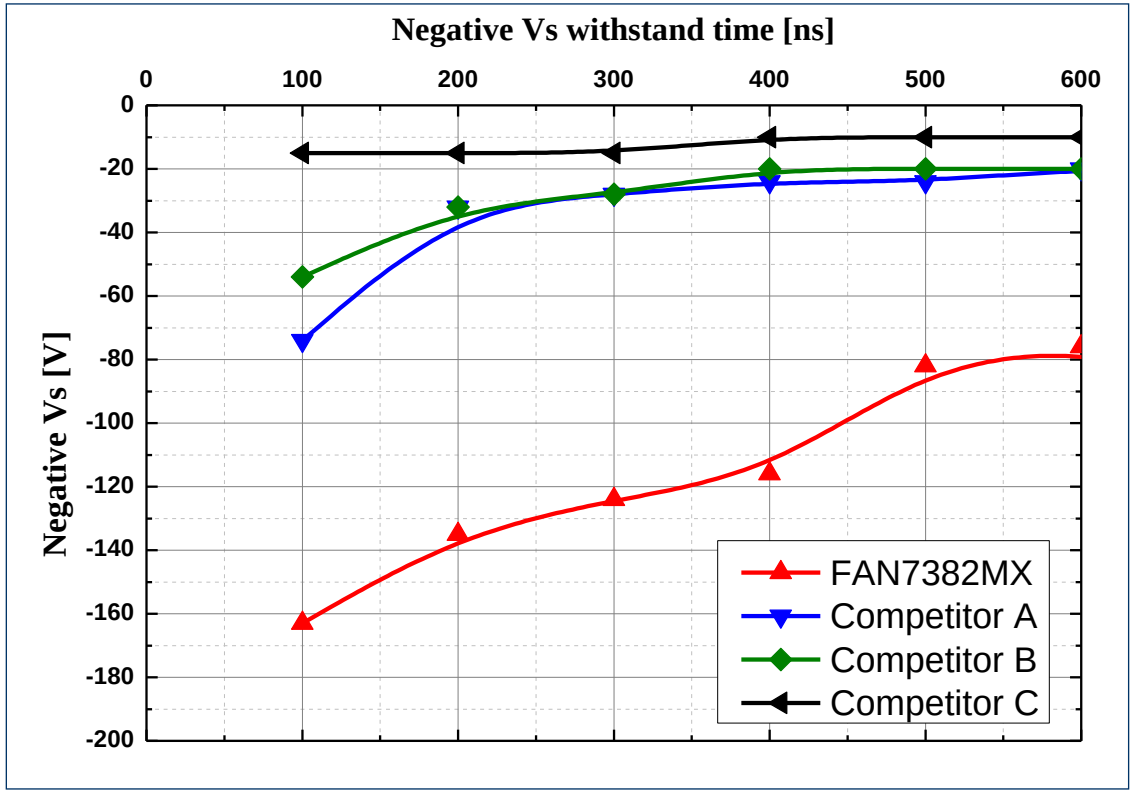
Typical -VS immunity curve - NPSOA

- Typical VS-NPSOA curves were made based on real test measurement value.
- Curve means malfunction or damage point of HVIC
- Onsemi HVIC shows better ruggedness of negative pulse VS than competitors.



< Typical VS-NPSOA >

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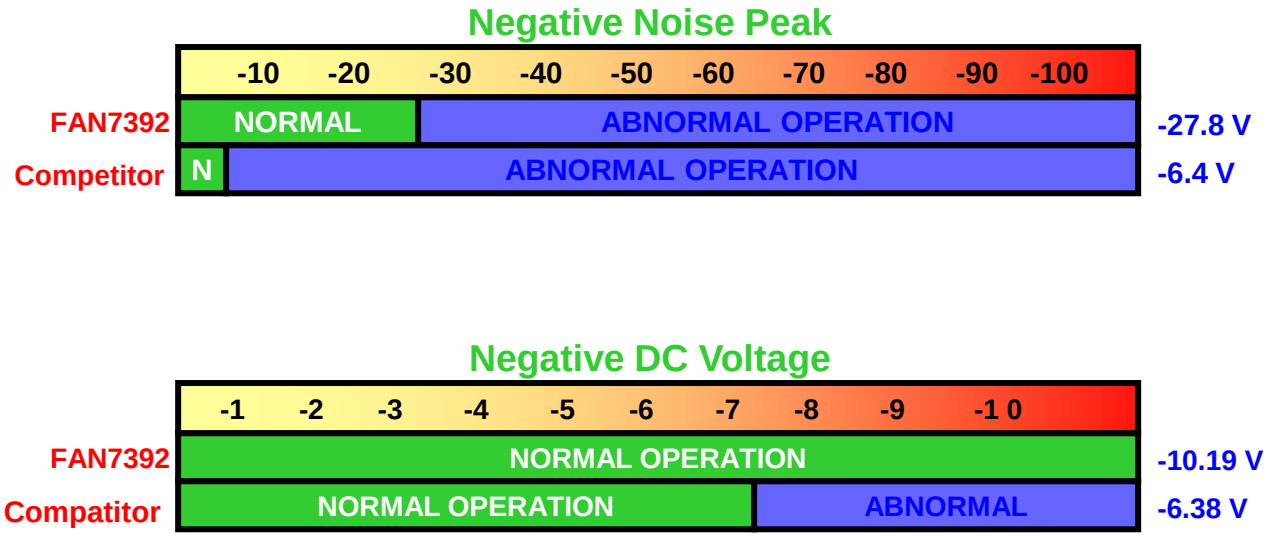
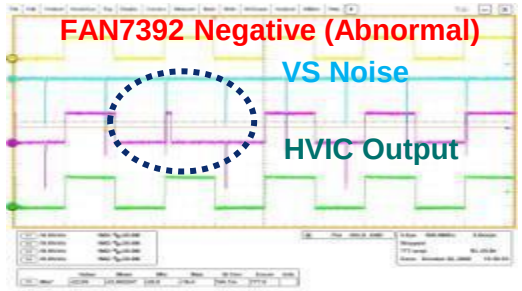
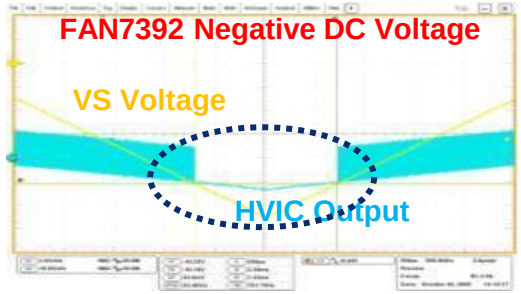
Results of Negative Vs Pulse & DC Level Test

- **Add Positive/Negative Noise on V_S**
  -. Negative : V_{DD}=15 V, V_{CC}=V_B=15 V, VS= 50ns, Positive/Negative Pulse Noise on V_S
- **Test Result**







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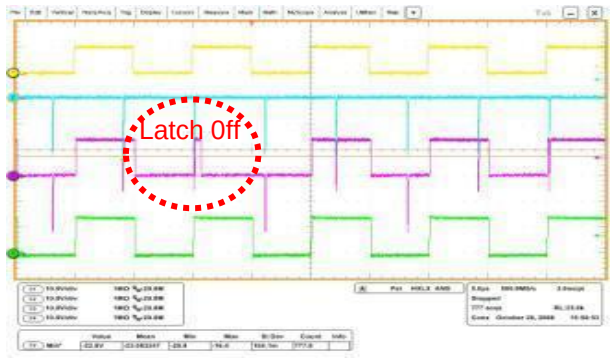
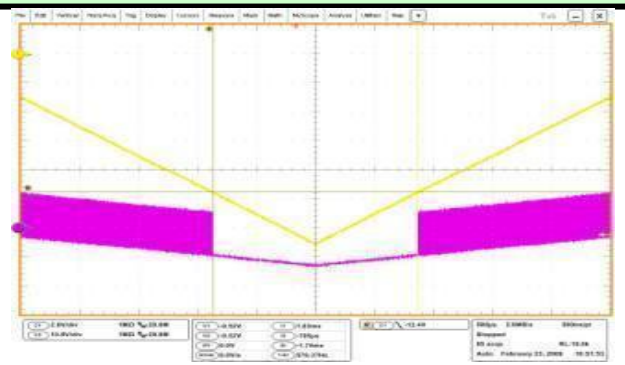
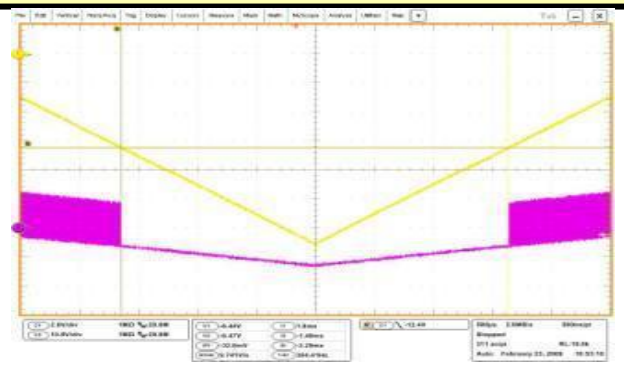
Waveforms of Negative Vs Pulse & DC Level Test

Pulse	FAN7392 -27.8 V		I-Company's A -6.4V	
V_{IN} [10V/div] V_S [10V/div] V_{HO} [10V/div] V_{LO} [10V/div]		Latch 0ff	V_{IN} [10V/div] V_S [10V/div] V_{HO} [10V/div] V_{LO} [10V/div]	 Missing
DC	**FAN7392 -10.19/-10.20V**		**I-Company's A -6.38/-6.40V**	
V_S [2V/div] V_{HO} [10V/div]			V_S [2V/div] V_{HO} [10V/div]	

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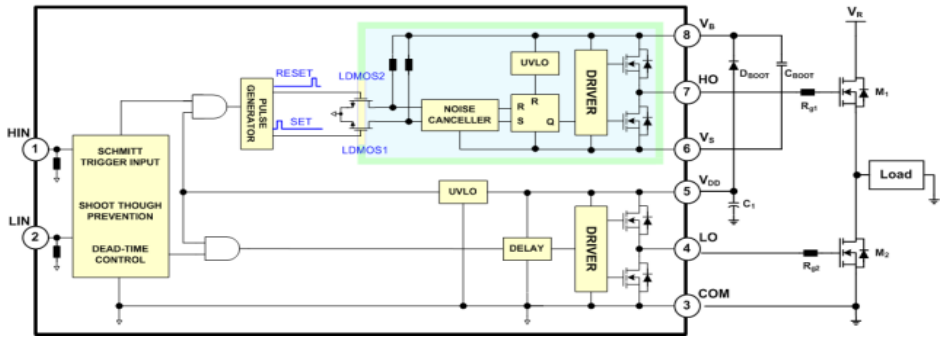
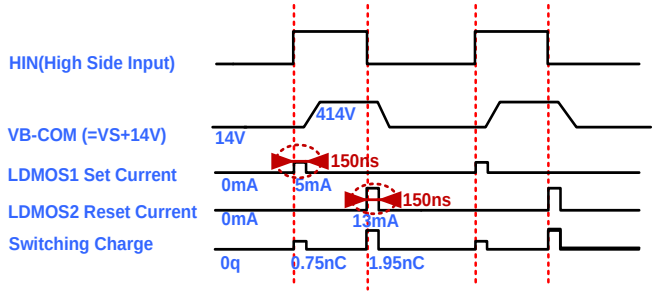
Waveforms of Negative Vs Pulse & DC Level Test

Block Diagram



Timing Chart



Equation

When Temp =25℃, V_{DD} = 15 V, V_{DBOOT} = 1 V, V_R = 400 V, Freq =100 kHz, T_{on}= 150 ns, I_d = 13 mA,

Set $Q_P = I_d \times T_{ON}$ = 5mA x 150ns = 0.75nC , *Reset $Q_P = I_d \times T_{ON}$ = 13mA x 150ns = 1.95 nC*

Set $P_D = (V_{DD}-V_{DBOOT}) \times Q_P \times Freq$= 14V x 0.75nC x 100KHz= 1mW , *Reset $P_D = (V_R+V_{DD}-V_{DBOOT}) \times Q_P \times Freq$= 414V x 1.95nC x 100KHz = 81mW*

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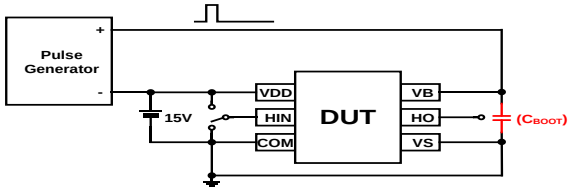
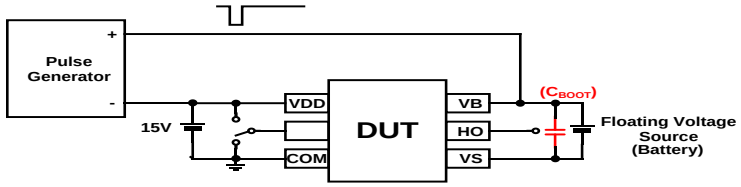
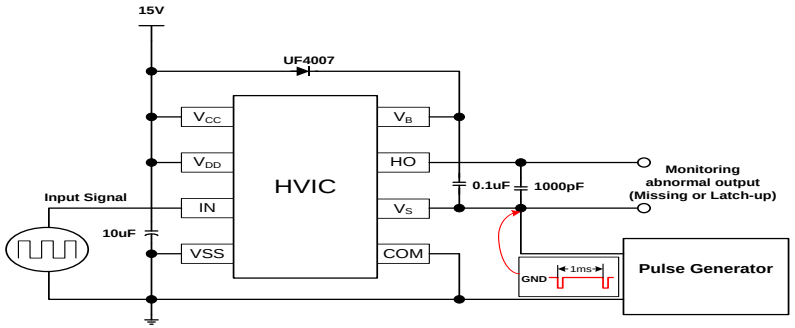
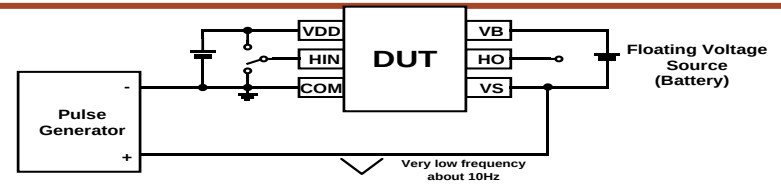
Appendix. HV IC Robustness Test Items

Items	Test Objective	Test Circuit
Positive V_B Pulse	Output status of the high-side driver is memorized by an internal latch circuit. The latch status must be only changed by input signal's rising and falling edges. However, a noise pulse applied to between V_B and V_S also can change the latch status. Such latch status change driven by the noise cause malfunction of HVIC. In general, it normally causes disastrous failure. Therefore, this test result gives h o w much the HVIC is robust against V_{BS} pulse noise.	
Negative V_B Pulse	When the V_B falls into negative voltage, high voltage junction is biased in forward direction. After that, even through V_B recovers positive voltage, current flows into the high voltage junction due to the reverse recovery phenomena, where the current amount is dependant on the charge builds up during forward bias, junction area and junction doping profile. These current flows are natural one. Therefore, it is impossible to stop such current flow. Unfortunately, these unwanted current flows causes abnormal operation of the HVIC.	
Negative V_S Pulse	When the negative voltage present at the source of the high-side switching device during turn-off causes load current to suddenly flow in the low-side freewheeling diode in half-bridge topology .This negative voltage can be serious trouble for the gate driver's output stage since it directly affects the source pin, which called Vs pin, of the gate driver and might pull some of the internal circuitry significantly below ground. Even though the peak duration is short, the magnitude can be higher than the break-down voltage of the high-side driver, which is given by process. Such unwanted high voltage stress can abnormally trigger the latch of the high-side driver. The another problem caused by the negative voltage transient is the possibility to develop an over voltage across the bootstrap capacitor. If the voltage of bootstrap capacitor exceed absolute maximum voltage rating by under shoot spike on Vs p i n , The gate drive IC will suffer damage.	
Allowable negative V_S DC	The high side output (HO) will not respond to input transitions like as signal missing problem while Vs undershoot condition. At this situation, the level shifter of the high side gate driver suffers from a lack of the operating voltage headroom. We can called that "Allowable negative V_S voltage ability for input signal propagation to output" and most of Fairchild HVIC has a allowable negative V_S pin voltage of at least -9.8V_{DC} at V_{BS}=15V.	

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Power Losses & Thermal considerations

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Brief look on losses

Static

- Low side quiescent current
- High side quiescent current
- High side to low side leakage current

Dynamic

- High side logic consumption
- Low side logic consumption
- Level shifter loss
- Charge and discharge external MOSFET, IGBT, etc.

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Brief look on losses

The Losses on one slide

Static losses: 1. Quiescent current from the positive voltage supply → $V_{CC} \cdot I_{QDD}$, $V_{boot} \cdot I_{Qboot}$
2. Leakage current from the high side to low side → $V_{BOOTpin} \cdot I_{HVleak}$

Dynamic losses: 1. Charge and discharge the gate of MOSFET → $V_{CC} \cdot Q_G \cdot f_{SW}$
there are two MOSFETS, multiple by 2
2. Operating for level shifter → $(V_{bulk} + V_{CC} - V_{Df\_boot}) \cdot Q_{set,reset} \cdot fsw$
3. Internal dynamic loss → $V_{CC} \cdot I_{CC}$, $V_{boot} \cdot I_{boot}$ without load condition

Bootstrap circuit loss: power loss on bootstrap diode and resistor during charging bootstrap capacitor and reverse bias power loss due to reverse recovery.

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Brief look on losses – NCV51511

- Condition: Temp =25℃, V_{DD} = 12 V, V_{DBOOT} = 1 V, VB = 80 V, Freq =100 kHz, Rg =0ohm, Q_G of external MOSFET = 80 nC

Item	Symbol	Equation	Calculation	Note
Static Loss at high side	$P_{D, q(HS)}$	$= V_{Boot} \times I_{LK}$	$= V_R \times I_{LK}$ = 80 V×0.3 µA = 2.4 µW (negligibility)	Calculated by leakage currents in the level shifting stage
Dynamic Loss on level shifter	$P_{D,sw(HS)}$	$= (V_R + V_{DD} - V_{DBOOT}) \times$ reset $Q_P \times f + (V_{DD} - V_{DBOOT}) \times$ set $Q_P \times f$	$= (V_R + V_{DD} - V_{DBOOT}) \times$ reset $Q_P \times f + (V_{DD} - V_{DBOOT}) \times$ set $Q_P \times f$ = (80 V + 12 V-1 V) × 0.48nC × 100 kHz + (12V-1V) X 0.48nC x 100kHz = 4.94 mW	Calculated by the level shifting circuit. (Q_p ; Charge for level shifting circuit) See the appendix for more info.
Quiescent current power Loss	$P_{D,q(LS)}$	$= V_{DD} \times (I_{QDD} + I_{QBS})$	$= V_{DD} \times (I_{QDD} + I_{QBS})$ = 12 V×(0.3+ 0.2) mA = 6 mW	Calculated by quiescent currents from the supplies voltage
Internal Dynamic Loss in	$P_{predriver}$	$= P_{predriver}$ $= V_{DD} \bullet (I_{PDD} + I_{PBS})$	$= V_{DD} \bullet (I_{PDD} + I_{PBS})$ = 12V × (0.3 + 0.4) mA = 8.4 mW	Dynamic losses associated internal pre-driver block See the datasheet
Gate driving Loss	P_G	$= 2xV_{DD} \times Q_G \times f$	$= 2xV_{DD} \times Q_G \times f$ = 2×12 V×80 nC×100 kHz = 192 mW	The losses in the gate drive resistance for charging external MOSFET (Q_G ; Total gate Charge of Switching Device)
Total Power Loss	P_{Total}	$= P_{D,q(HS)} + P_{D,q(LS)} + P_{D,SW(HS)} + P_{predriver} + P_G$ = 4.94+6+8.4+192= **211.34 mW**		

In NCV51511, the main power loss is dynamic losses for charging/discharging FET.

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Brief look on losses – NCV51511 Thermal Analysis

- Power dissipation = 211.34 mW.
- If $\boldsymbol{\theta_{JA}}$ and Ta are given
  $Tj = Pd \cdot \theta_{JA} + Ta = 0.21 \cdot 39 + Ta = 8.19 + Ta$ (°C)
- If $\boldsymbol{\Psi_{JL}}$ is known and can measure lead temperature (T_{Lead})
  $Tj = Pd \cdot \Psi_{JL} + T_{Lead} = 0.21 \cdot 15 + T_{Lead}$ °C $= 3.15 + T_{Lead}$ (°C)
- If $\boldsymbol{\Psi_{JT}}$ is known and can measure case-top temperature (T_{Top})
  $Tj = Pd \cdot \Psi_{JT} + T_{Top} = 0.21 \cdot 6 + T_{Top}$ °C $= 1.26 + T_{Top}$ (°C)

Junction temperature (Tj) should be controlled within the recommended operating temperature range

If Tj is over than recommended operating temperature

1. Add external gate resistors to share the thermal distribution
2. Reduce switching frequency
3. Use heat sink

Table 4. THERMAL INFORMATION (Note 4)

Symbol	Parameter	Value	Units
θ_{JA}	Thermal Resistance Junction–Air (Note 4)	39	°C/W
ψ_{JL}	Thermal characterization parameter Junction–Lead	15	°C/W
ψ_{JT}	Thermal characterization parameter Junction–Case (TOP)	6	°C/W

4. As mounted on a 76.2 x 114.3 x 1.6 mm FR4 substrate with a Multi–layer of 1 oz copper traces and heat spreading area. As specified for a JEDEC 51–7 conductivity test PCB. Test conditions were under natural convection or zero air flow

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Brief look on losses

NCV51511

- Package SOIC8 EP
- Rtja = 39 K/W
- Ploss = 211 mW
- tj (@ amb = 60 °C) = 68.2 °C

NCV5183

- Package SOIC8
- Rtja = 183 K/W
- Ploss = 209 mW
- tj (@ amb = 60 °C) = 98 °C

The exposed pad decreases junction temperature by 30 °C

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Quick tool for HVIC Drivers Loss & Thermal estimation

AND90004 : Analysis of Power Dissipation and Thermal Considerations for High Voltage Gate Drivers

(and PD calculator is linked in each devices' landing page 'Design & Development Tools')

Analysis of Power Dissipation and Thermal Considerations for High Voltage Gate Drivers

AND90004/D

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APPLICATION NOTE

Gate drivers used to switch MOSFETs and IGBTs at high frequencies can dissipate significant amount of power depending on the operating conditions. It is important to determine the driver power dissipation and the resulting junction temperature in the application to ensure that the part is operating within acceptable temperature limits. High voltage gate drive IC (HVIC) is high side and low side gate drive IC designed for high−voltage, high−speed driving MOSFET for a half bridge switching application. Figure 1 shows the typical internal block diagram of HVIC. The main function blocks are the input stage, UVLO protections, level shifter and output driver stages. The gate driver losses include:

- Static losses related with static current at high and low side circuit blocks when driver is biased and not switching.
- Dynamic losses related with dynamic current when the switching signal is applied so linked to switching frequency.
- Gate driving losses related with load switch charges and also directly dependent on switching frequency.

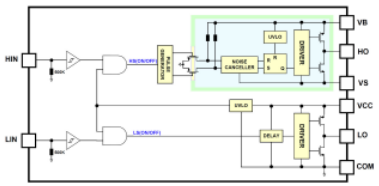

Figure 1. Block Diagram of HVIC

The bootstrap diodes losses will not be discussed in this document because the current flowing the diode will be included in dynamic losses. However, one thing not to be overlooked is the instantaneous power loss to charge the bootstrap capacitor during start up. During this time a significant current can flow through the diode to quickly charge the bootstrap capacitor and can generate relatively high losses during several switching periods. The bootstrap diode must withstand this current and power loss and this loss will add to driver internal power losses when this diode is.

Static Power Loss Analysis

The Figure 2 shows a simplified schematic of the half bridge switch network associated with high and low side driver to explain the static losses.

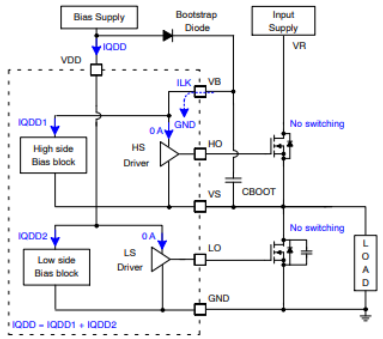

Figure 2. Simplified Circuit Diagram of Driver and Half−bridge Configuration for Static Power Losses

The static losses are due to the quiescent currents from dc voltage supplies V_{DD} to ground in the low−side driver and the leakage current in the level shifter in the high−side driver as described by the following equations.

$$P_{Static} = P_{Quiescent} + P_{Leakage} \quad \text{(eq. 1)}$$

$$P_{Quiescent} = V_{DD} \times I_{QDD} \quad \text{(eq. 2)}$$

$$P_{Leakage} = (V_R + V_{BOOT}) \times I_{LK} = (V_R + V_{DD} - V_{DBBOOT}) \times I_{LK} \quad \text{(eq. 3)}$$

Where, I_{QDD} is the quiescent current of V_{DD} supply under no input switching signal, V_{BOOT} is charged voltage on C_{BOOT}, V_{DBOOT} is the forward voltage drop on bootstrap diode, V_R is the rail voltage from input supply and I_{LK} is the leakage current at boot pin (VB pin in Figure 2). The static

Gate Driving Loss Analysis

The gate driving loss in the driver is the most significant power loss resulting from supplying gate current to switch the load MOSFET *On* and *Off* at the switching frequency. The gate driving losses are coming from charging and discharging the load capacitor (for MOSFET, the load capacitor is the input capacitor of MOSFET) and expressed by the following equation.

$$P_{charging} = P_{discharging} = 0.5 \times V_{DD} \times Q_g \times f_{sw} \quad \text{(eq. 8)}$$

Where, Q_g is the total gate charge of the external MOSFET and f_{sw} denotes the switching frequency. In case of a soft switching topology, Q_g is equal to gate to source charge (Q_{gs}) of the FET or IGBT. The total gate driving losses in high and low side drivers is then 4 times $P_{charging}$.

$$P_{gate\_driving} = 2 \times V_{DD} \times Q_g \times f_{sw} \quad \text{(eq. 9)}$$

Since the major power loss is the gate driving loss, the simplest and fastest way to calculate the losses in a driver is to sum the gate driving loss (P_{gate_drving}) and dynamic losses on V_{DD}.

These losses acount for more than 90% in recent middle voltage class high and low side driver products.

Thermal Analysis

Once the power dissipated inside the driver is calculated, we can estimate the junction temperature of the driver. This can be evaluated assuming thermal resistance or characterization was determined for a similar thermal design (heat sinking and air flow). The thermal equation is:

$$T_J = P_{TOTAL} \times R_{jx} + T_x \quad \text{(eq. 10)}$$

Where:

T_J = the junction temperature of driver die

R_{jx} = thermal resistance (θ) or characterization parameter (Ψ) relating temperature rise to total power dissipation

T_x = temperature of point x as defined in the thermal characteristic table from datasheet.

The thermal information is shown in Figure 5 and Table 1. Thermal characteristic of the package is a function of several parameters such as geometry, boundary condition, test condition, etc. This requires numerical analytical tool or modeling technique that are generally cumbersome to manipulate. It can be tricky to estimate the junction temperature precisely with thermal information coming from datasheet.

So it is helpful to review the definition of thermal information.

1. θja is the Junction−to−Air Thermal Resistance. It measures theheat flow between the die junction and the air. It is mainly relevant for packages used without any external heat sink.
2. θjc is the Junction−to−Case Thermal Resistance and it measures the heat flow between the die junction and the surface of the package. It is mainly relevant for packages using some external heat sinks
3. Ψjt is the Junction−to−PKG Top Thermal Characterization Parameter and it provides correlation between die temperature and temperature of package topside. This can be used to estimate die temperature in applications
4. Ψjb is the Junction−to−Board Thermal Characterization Parameter and it provides correlation between die temperature and board temperature. This can be used to estimate die temperature in applications.

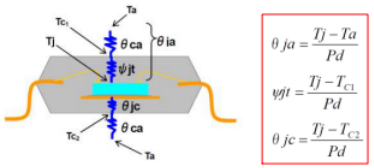

Figure 5. Thermal Resistance and Characterization Parameters with Package

Table 1. DEFINITION OF THERMAL RESISTANCE AND CHARACTERIZATION PARAMETERS

Item	Definitions
θja	Thermal resistance between Tj and Ta
Ψjt	Thermal characterization parameter between Tj and T_{C1}
θjc	Thermal resistance between Tj and T_{C2}
θca	Thermal resistance between Tc and Ta
Tj	Junction temperature
Ta	Ambient temperature
T_{C1}	Temperature of the top surface of IC package
T_{C2}	Temperature of the bottom surface of IC package
Pd	Maximum permissible powe

Generally, the thermal information provided in semiconductor datasheet can't cover all applications cases. For the following examples we'll only use θja for Tj calculation.

For more details on how to properly use thermal data found in datasheet, please refer to detailed Application notes: www.onsemi.com/pub/Collateral/AND8220−D.PDF.

Recommendations to Reduce T_j

In case Tj is too close to the recommended operating temperature, there are few things that could be considered.

1. Add external gate resistors to distribute the power losses: When no external gate resistor is inserted between the driver and MOSFET, the power is entirely dissipated inside the driver package. Using external gate resistor allows to share the power

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Tools and Generic Help

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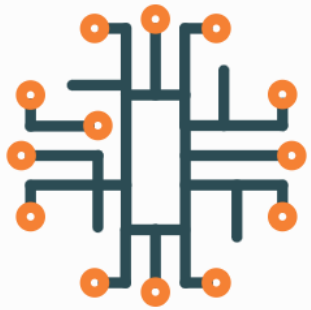

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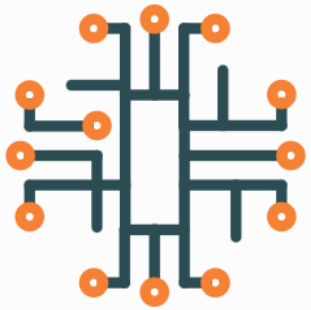

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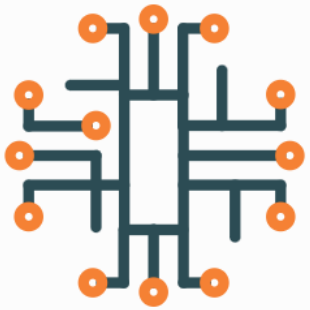

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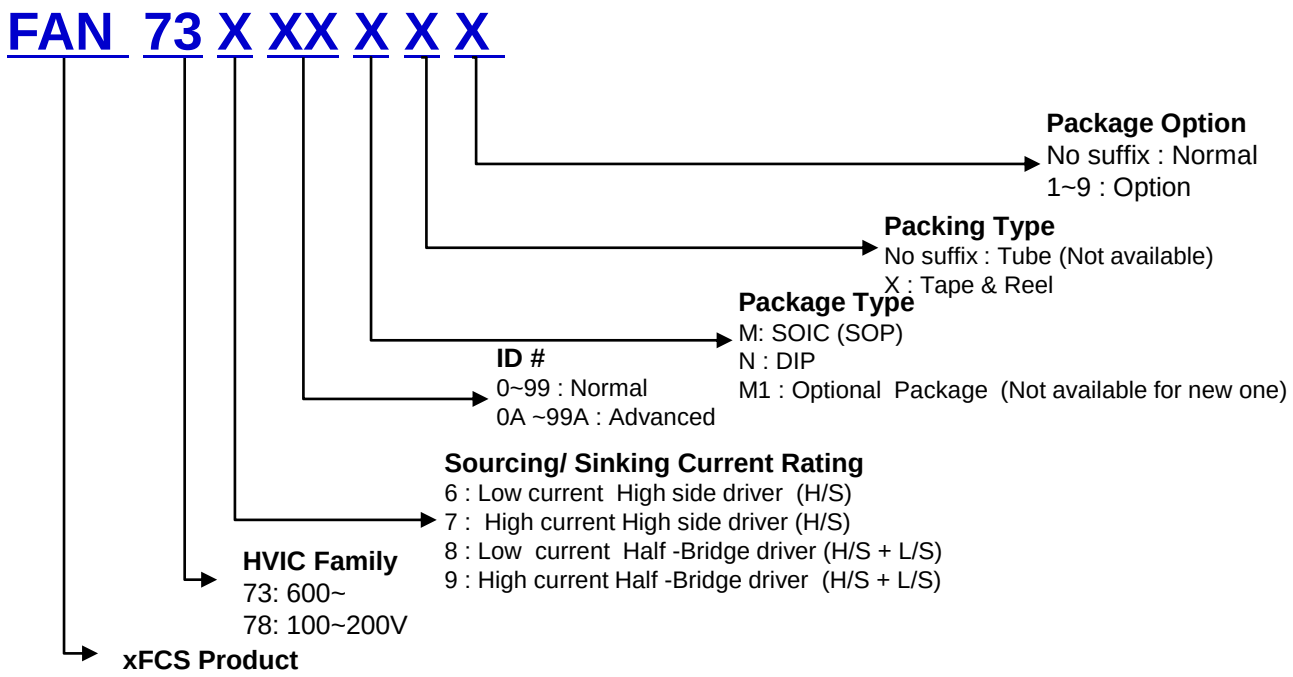
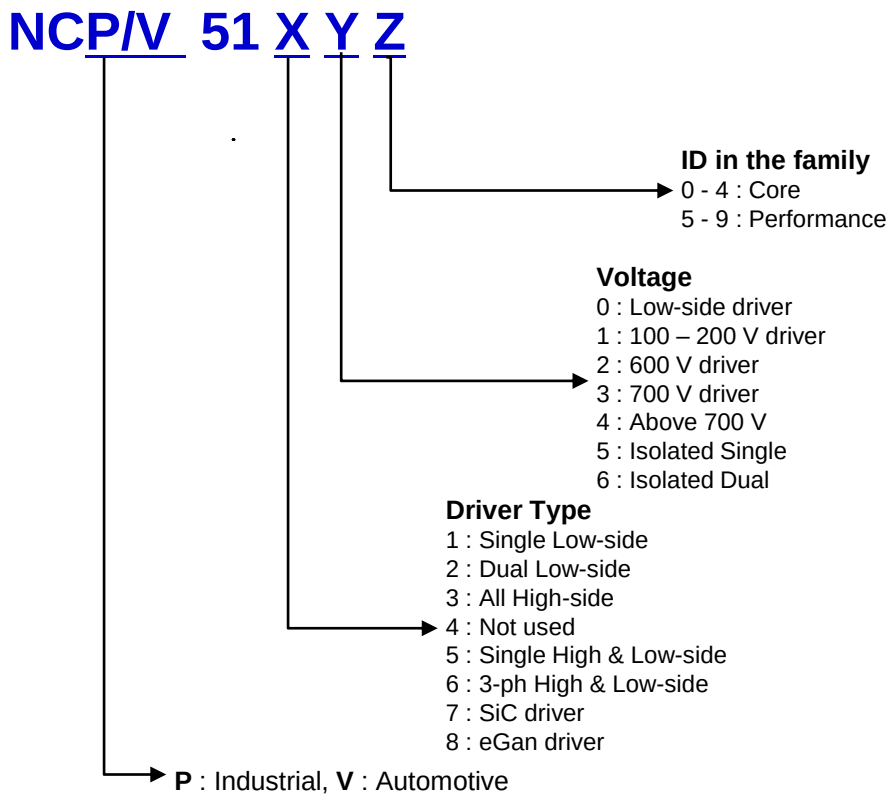
Nomenclature





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High Voltage Gate Driver Products

Type	Product	In - Out	Offset Voltage (V)	Output Current		Delay Time		Shut Down	OCP	DT/IL (ns)	PKG
				SRC (mA)	SNK (mA)	Ton (ns)	Toff (ns)				
High-Side Only	FAN7361/2	1 to 1	600	250	500	120	90	No	No	No	8SOP
	FAN73611	1 to 1	600	250	500	120	120	No	No	No	8SOP
	FAN7371/ 73711	1 to 1	600	4000	4000	150	150	No	No	No	8SOP
	FAN7385	2 to 2	600	350	650	110	110	No	No	No	14SOP
	NCP51313A/B	1 to 1	200	5000	5000	65/25	65/25	No	No	No	DFNW6
High & Low-Side	FAN7382	2 to 2	600	350	650	170	200	No	No	No	8SOP, 14SOP
	FAN7390A	2 to 2	600	4500	4500	140	140	No	No	No	14SOP
	FAN73901	2 to 2	600	2500	2500	140	140	No	No	No	8SOP
	FAN7391	2 to 2	600	4500	4500	150	150	No	No	No	14SOP
	FAN73912A	2 to 2	1200	2000	3000	500	550	Yes	No	No	16 WSOP
	FAN7392	2 to 2	600	3000	3000	130	150	Yes	No	No	16 WSOP
	FAN7842	2 to 2	200	350	650	170	200	No	No	No	8SOP
	FAN8811 (NCV51511)	2 to 2	100	3000	6000	30	28	No	No	No	10WDFN (8SOP-EP)
	NCP5106A	2 to 2	600	250	500	100	100	No	No	No	8SOP, 10DFN
	NCP5109A	2 to 2	200	250	500	100	100	No	No	No	8SOP, 10DFN
	NCP5181	2 to 2	600	1400	2200	100	100	No	No	No	8DIP, 8SOP
	NCP5183	2 to 2	600	4300	4300	120	120	No	No	No	8SOP
	NCP51530A/B	2 to 2	700	3500	3000	60/25	60/25	No	No	No	8SOP, 10DFN
	NCP51513xA	2 to 2	130	2000	3000	20	20	Yes	No	0/No	DFN10 3x3
Half Bridge	FAN7380	2 to 2	600	90	180	135	130	No	No	100	8SOP
	FAN7383	1 to 2	600	350	650	500	170	Yes	No	Variable	14SOP
	FAN7387	1 to 2	600	350	650	550	160	Yes	No	Variable	8SOP
	FAN73832	1 to 2	600	350	650	580	180	Yes	No	Variable	8SOP
	FAN73833	2 to 2	600	350	650	150	140	No	No	450	8SOP
	FAN7384	2 to 2	600	250	500	180	170	Yes	Yes	120	14SOP

Type	Product	In - Out	Offset Voltage (V)	Output Current		Delay Time		Shut Down	OCP	DT (ns)	PKG
				SRC (mA)	SNK (mA)	Ton (ns)	Toff (ns)				
Half Bridge	FAN73912	2 to 2	1200	2000	3000	500	550	Yes	No	330	16 WSOP
	NCP51513xB	2 to 2	130	2000	3000	50	50	No	No	80	DFN10 3x3
	FAN7393A	1 to 2	600	2500	2500	530	130	Yes	No	Variable	14SOP
	FAN73932	1 to 2	600	2500	2500	600	200	Yes	No	400	8SOP
	FAN73933	2 to 2	600	2500	2500	160	160	No	No	Variable	14SOP
	FL73282	2 to 2	900	350	650	150	150	No	No	170	8SOP
	NCP1392B	1 to 2	600	500	1000	N/A	N/A	No	No	610	8SOP
	NCP1392D	1 to 2	600	500	1000	N/A	N/A	No	No	305	8SOP
	NCP1393B	1 to 2	600	1000	1500	N/A	N/A	No	No	610	8SOP
	NCP5104	1 to 2	600	250	500	620	100	Yes	No	520	8DIP, 8SOP
	NCP5106B	2 to 2	600	250	500	100	100	No	No	100	8SOP,10DFN
	NCP5109B	2 to 2	200	250	500	100	100	No	No	100	8SOP, 10DFN
	NCP5111	1 to 2	600	250	500	750	100	No	No	650	8DIP, 8SOP
	NCP5304	2 to 2	600	250	500	100	100	No	No	100	8DIP, 8SOP
3-Phase Half-Bridge	FAN7388	6 to 6	600	350	650	130	150	No	No	270	20SOP
	FAN73893/ FAN73894	6 to 6 (inverting)	600	350	650	500	500	Yes	Yes	320	28SOP
	FAN73895/ FAN73896	6 to 6	600	350	650	500	500	Yes	Yes	320	28SOP
	FAN7888	6 to 6	200	350	650	130	150	No	No	270	20SOP
WBG	NCP51705	1 to 1	-	6000	6000	25	25	Yes	Yes	Adj	24QFN
	NCP51810	2 to 2	150	1000	2000	25	25	Yes	No	Adj	15QFN
	NCP51820	2 to 2	650	1000	2000	25	25	Yes	No	Adj	15QFN

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