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Gate Drive System for Silicon Carbide Power Modules in Automotive Traction Application

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Introduction

The recent trend in the automotive industry is towards electrification of the vehicles. Efficiency is one of the key parameters for battery electric vehicles since higher efficiency translates to increased range for the vehicles, reduced weight and cost due to the reduction of batteries in the vehicle. Silicon carbide MOSFET is the technology which enables increase in the efficiency of the electric powertrain. The gate driver used to drive the power module is a very important component of the traction inverter. A good design of the gate driver is essential for obtaining high efficiency of the inverter as well as ensuring the safety of the inverter.

As part of this work, a three−phase gate driver board SEC−SiCGDSSDC−GEVB is designed with a new isolated gate driver IC from onsemi, which is NCV57050. NCV57050 meets all the requirements of a complete gate drive for SiC modules. Some of the features of NCV57050 are very high drive current capability, fast DESAT protection, other protection features, isolated temperature measurement, active miller clamp, wide bias voltage range etc.

This application note covers the specification, design, and test results of SEC−SiCGDSSDC−GEVB evaluation board, which is shown in Figure 1 and Figure 2. This gate driver board demonstrates a complete gate driver solution for the Single side Direct Cooling 6−pack Silicon Carbide Power Module (SSDC Module) shown in Figure 3.

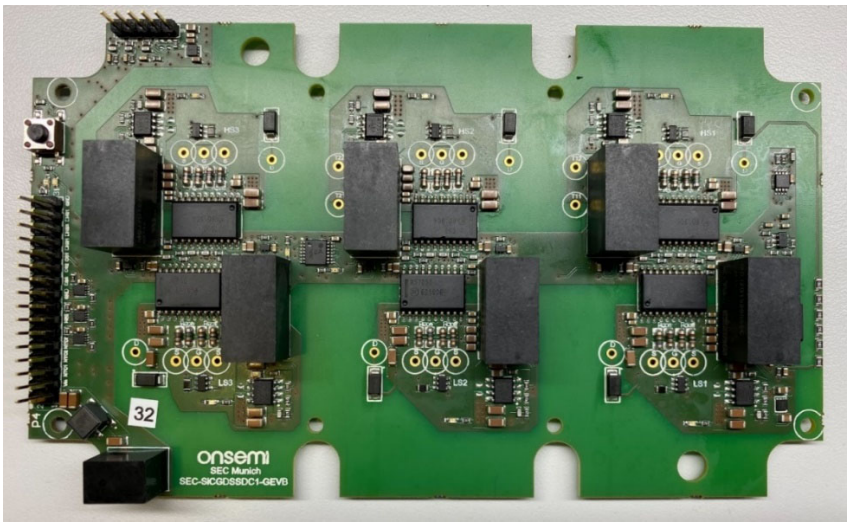

Figure 1. SSDC SiC Gate Driver Top View

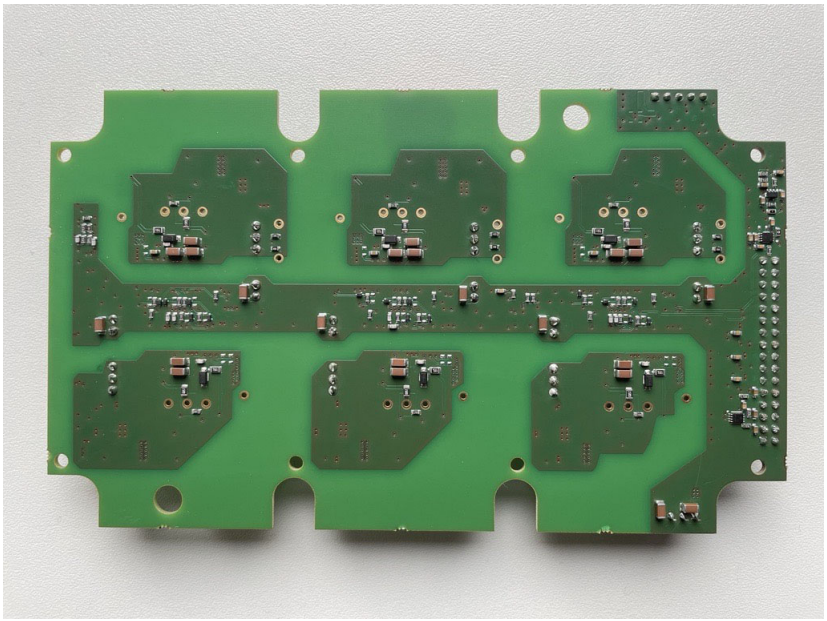

Figure 2. SSDC Gate Driver Bottom View

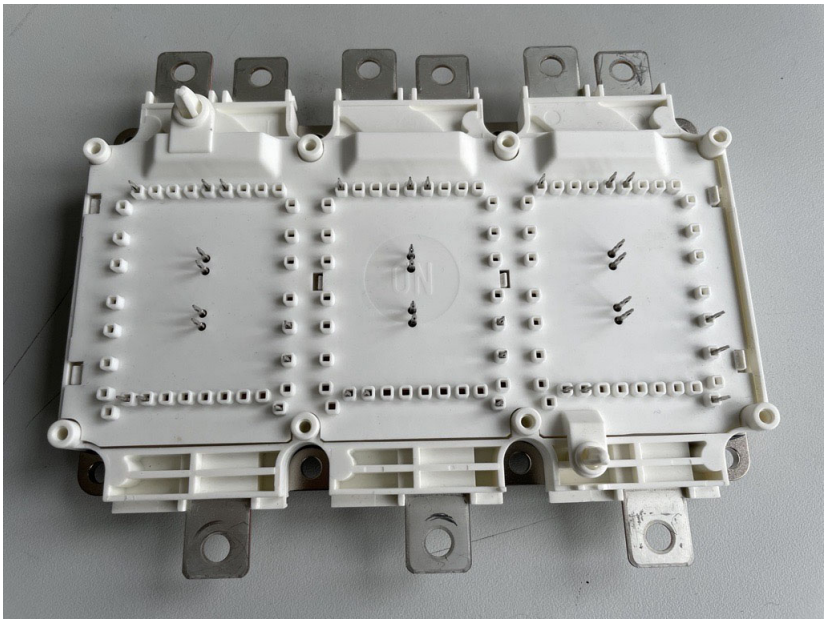

Figure 3. SSDC SiC Power Module

Applications

- Main Traction Inverter for Battery Electric Vehicle, Plug−in Hybrid Vehicles, and Full Hybrid Vehicles

Features of NCV57050

- Galvanic Isolation

- High driver current output
- Cross conduction protection
- Active miller clamp for fast swtiching
- DESAT OC protection
- Soft turn−off during short circuit condition
- High CMTI
- Over temperature protection
- Open drain FAULT and READY outputs

System Overview

The powertrain for automotive applications consists of a 3−phase inverter and motor, connected to HV batteries through a dc link capacitor. A controller generates the PWM signals needed to control the inverter and the gate driver receives these PWM signals from the controller and generates the gate source voltages required to drive the switches of the inverter, as shown in Figure 4.

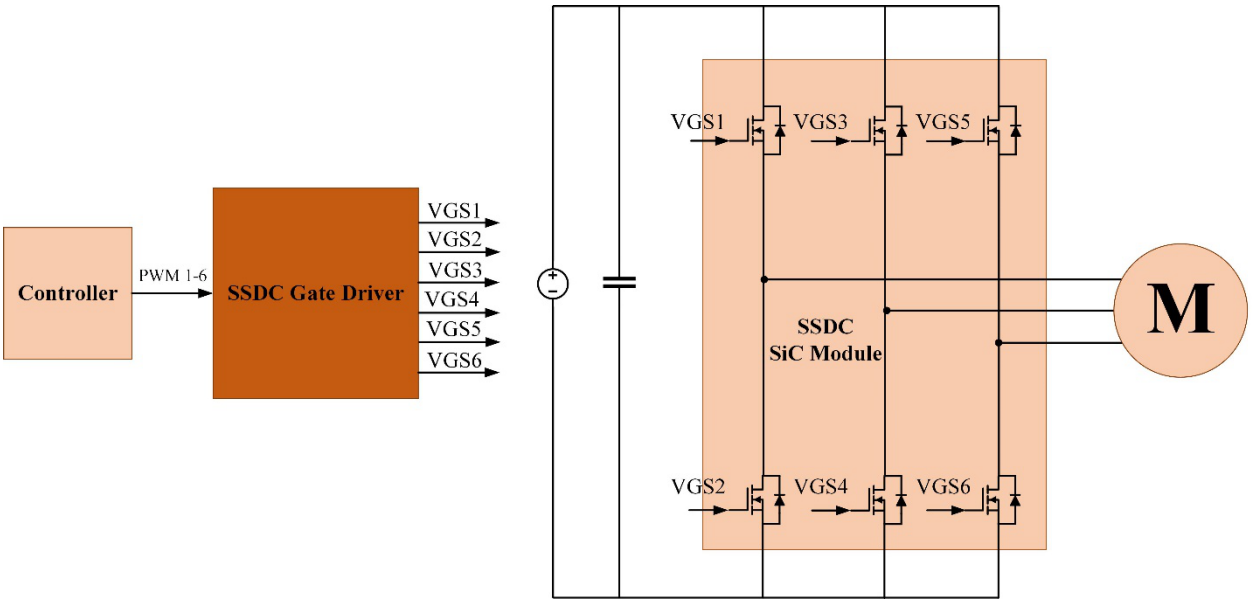

Figure 4. Traction Inverter System

For the simplicity of understanding, from here on, the driver IC NCV57050 will be referred to as NCV57050 or gate driver, and the three−phase gate driver evaluation board is called as gate driver board. The gate driver system (for a single half bridge) consisting of multiple function blocks is shown in Figure 5.

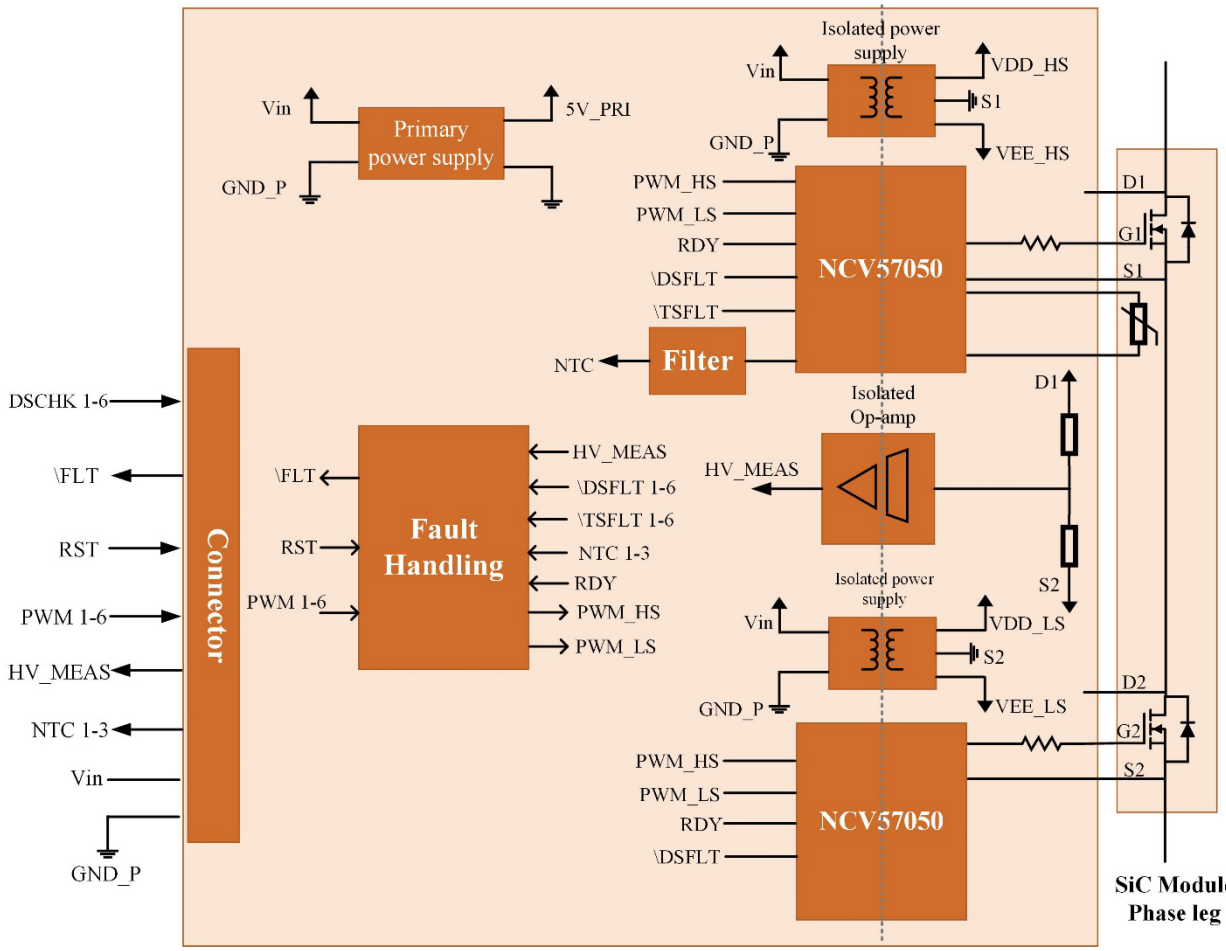

Figure 5. Block Diagram of Gate Driver Board

The left most block called “Connector” is used to interface the gate driver board with the controller. The “Fault Handling” block ensures the safe start of the gate driver and safety of the system in case of any faults. The gate drive block “NCV57050” is responsible for driving the MOSFETs in the module and for providing galvanic isolation between LV and HV side. Since NCV57050 IC is a single channel gate driver each MOSFET requires its own driver IC. Each NCV57050 gate driver block is powered by an “Isolated power supply” which generates the VDD, and VEE voltage required for driving the SiC devices. The temperature of the module is sensed by NCV57050 using the NTCs present in the SSDC module. DC link voltage is measured with an isolated Op−amp on the gate driver board.

Specification and Operation Conditions

The specification and main features can be seen in the Table 1.

Table 1. GATE DRIVER EVALUATION BOARD SPECIFICATIONS

Parameter	Symbol	Value
Supply Input		
Input Voltage for the gate driver	V_{in}	15 V
DC link voltage for power module	V_{dclink}	0−500 V
Digital Inputs		
PWM signals for switches	PWM1..PWM6	CMOS Level
Switching Frequency of input PWM	F_{sw}	Max. 16 kHz
Reset signal after powerup and to reset fault latch	RST_CTRL_SIG	CMOS Level
DESAT check signals	DSCHK1...DSCHK6	CMOS Level
Digital Outputs		
Fault state indicator	FAULT	CMOS level
Fault latch state indicator	LATCH_FLT	CMOS level
Analog Outputs		
NTC resistance measurement	NTC_MEAS1...NTC_MEAS3	0−5 V
DC Link voltage measurement	HV_MEAS	0−5 V
Gate Drive Voltage		
On state gate drive voltage	VDD	18 V
Off state gate driver voltage	VEE	−5 V

Remark: CMOS level: V_{IH} = 3.5 V − 5 V, V_{IL} = 0 V− 1.5 V

Design

Considerations for the design of each of the blocks of the gate driver system are described below.

Isolated Power Supply

A regulated galvanically isolated power converter is crucial for proper turn−on and turn−off the MOSFETs. The power supply provides power to switch the MOSFETs on and off during operation. The exact voltages required to turn−on and turn−off is determined by the technology of the MOSFET. In general, increasing the gate voltage during the ON−state reduces the R_{DSon} of the MOSFET which in−turn helps in reducing the conduction losses of the system. A negative gate voltage during its off state is highly recommended for fast switching, dv/dt immunity and to reduce the leakage current. In this gate driver, the ON−state voltage and the OFF−state voltage are designed to be 18 V and −5 V respectively. The architecture of the power supply on this gate driver is as shown in Figure 6. It consists of a galvanically isolated DC−DC converter which generates output voltages of 20 V and −5 V. An LDO then regulates the 20 V down to 18 V.

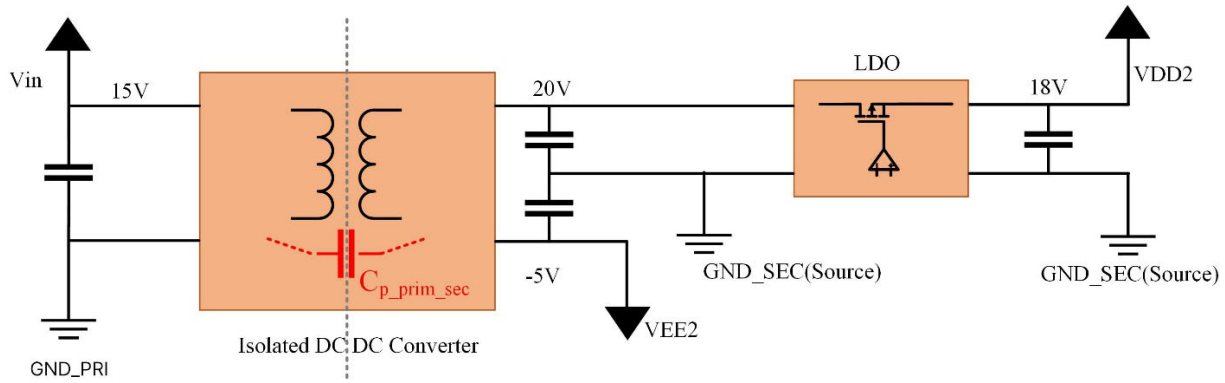

Figure 6. Power Supply

While selecting the isolated DC−DC converter following considerations are important:

Power Requirement

The DC−DC converter should be capable of providing sufficient power to switch the MOSFETs at maximum switching frequency of the inverter. In this design, the power required to drive the gates of the SiC module can be calculated as

$$P_{gate} = \Delta V_{GS} \times Q_G \times F_{sw} = 1.1\ W \qquad \text{(eq. 1)}$$

Where, ΔV_{GS} = 18−(−5) = 23 V is the gate source voltage difference

Q_G = 2.4 μC is the gate charge for SSDC module (NVXR17S90M2SPB)

F_{sw_max} = 16 kHz is the maximum switching frequency

Furthermore, the DC−DC converter also powers the secondary side of the gate driver IC NCV57050 and must also provide for the LDO losses. Therefore, the rated power of the DC−DC converter should meet the condition

Rated power > Gate drive losses + LDO losses + NCV57050 secondary bias power.

Galvanic Isolation

Galvanic isolation between the LV and HV side of the circuit is required for safe operation of the system. Furthermore, due to the separation of the ground on the low voltage and the high voltage side, the ground loop problem of the gate driver is avoided. Therefore, the power supply should have a reinforced isolation between its primary and secondary side for the maximum DC link voltage in the system. In this application the maximum DC link voltage is expected to be 500 V.

High Common Mode Transient Immunity (CMTI)

SiC MOSFETs are capable of switching voltages and currents faster than silicon MOSFETs or IGBTs. Due to the high dv/dt during the switching, currents are injected from the secondary side to the primary side through the coupling capacitance of the power supply. If the currents are very high, disturbance created can interfere with the system and result in malfunction.

Therefore, it is very important to minimize the coupling capacitance ($C_{p\_prim\_sec}$, as shown in Figure 6.) between the primary and secondary side to achieve high CMTI. In traction application, it is common to have dv/dt in the range of 10 V/ns to 20 V/ns.

Based on this, the isolated power supply MGJD152005SC from Murata is selected which has a rated output power of 2 W and a typical coupling capacitance of only 3 pF and a minimum CMTI rating of 100 V/ns.

Gate Drive with NCV57050

Peak Gate Current Requirement

During the turn−on and turn−off of a MOSFET, the gate driver charges and discharges the gate of the MOSFET. The gate drive currents charging and discharging various capacitances of the MOSFET are as shown in Figure 7. For fast switching of the MOSFETs, the gate driver should be capable of sourcing and sinking high currents.

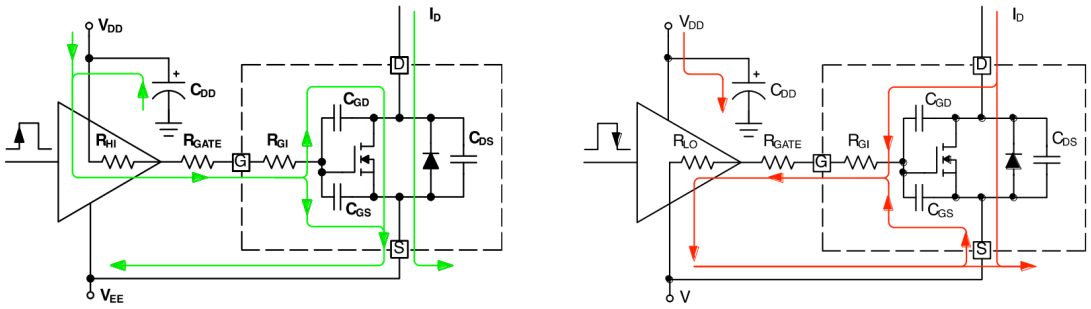

Figure 7. Gate Drive Current Paths during Turn−on and Turn−off

A SiC power module switch consists of multiple MOSFET dies connected in parallel for high current applications. Therefore, a very high current is required from the gate driver to achieve switching speeds required to obtain high efficiencies. If the gate driver is unable to supply such high currents, an additional current buffer stage is typically used in between the gate driver and the MOSFET to increase the current as shown in Figure 8.

However, the gate driver IC NCV57050 has very high peak source and sink currents of 15 A which is sufficient to achieve high turn−on and turn−off speeds for the SSDC module. Therefore, in this design an additional current buffer stage is not used. This has the advantage of reducing the BOM cost of the design and simplifies the PCB design. The drive stage of this gate driver is as shown in Figure 9.

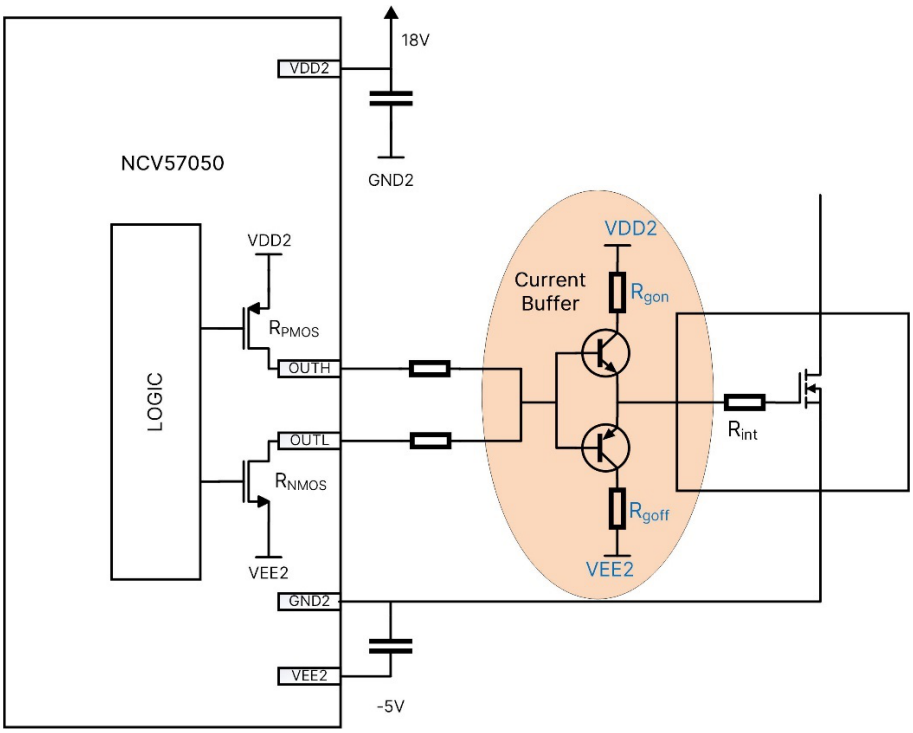

Figure 8. Gate Drive Stage with Current Buffer

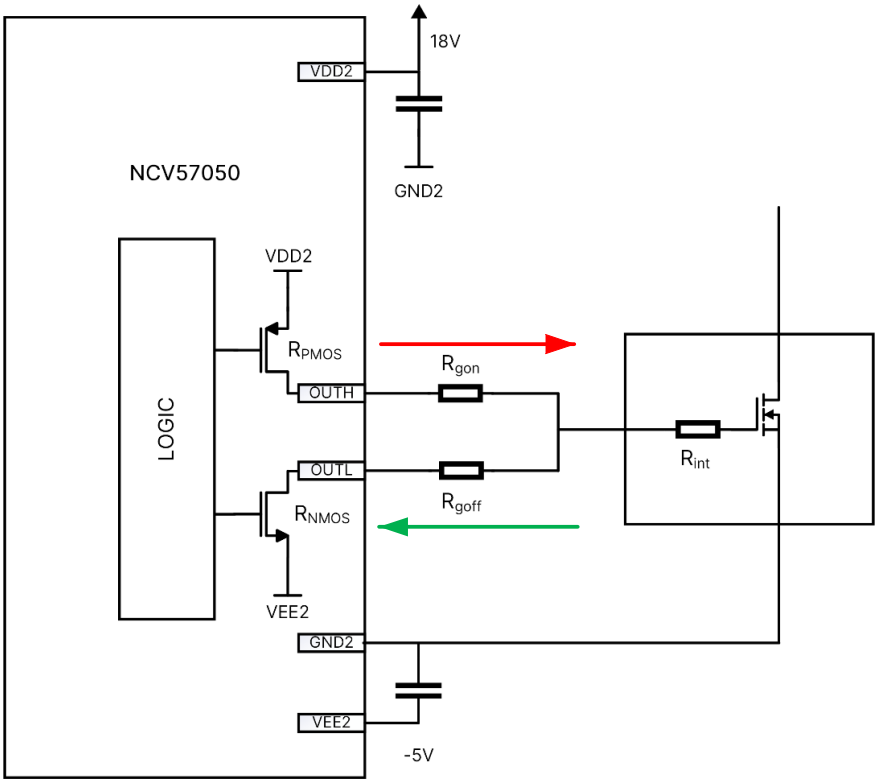

Figure 9. Gate Drive Stage with NCV57050 (without Current Buffer)

PCB Layout Recommendations for Gate Loops

While designing the PCB layout, there are a few important considerations. The decoupling capacitors and the bulk capacitors of NCV57050 should be dimensioned with care and should also be placed as close as possible to the pins of NCV57050. The bulk capacitors store the energy needed to drive the gates. Due to the high peak source and sink gate currents, at least 30 μF capacitance should be used as bulk capacitance for VDD2 and VEE2.

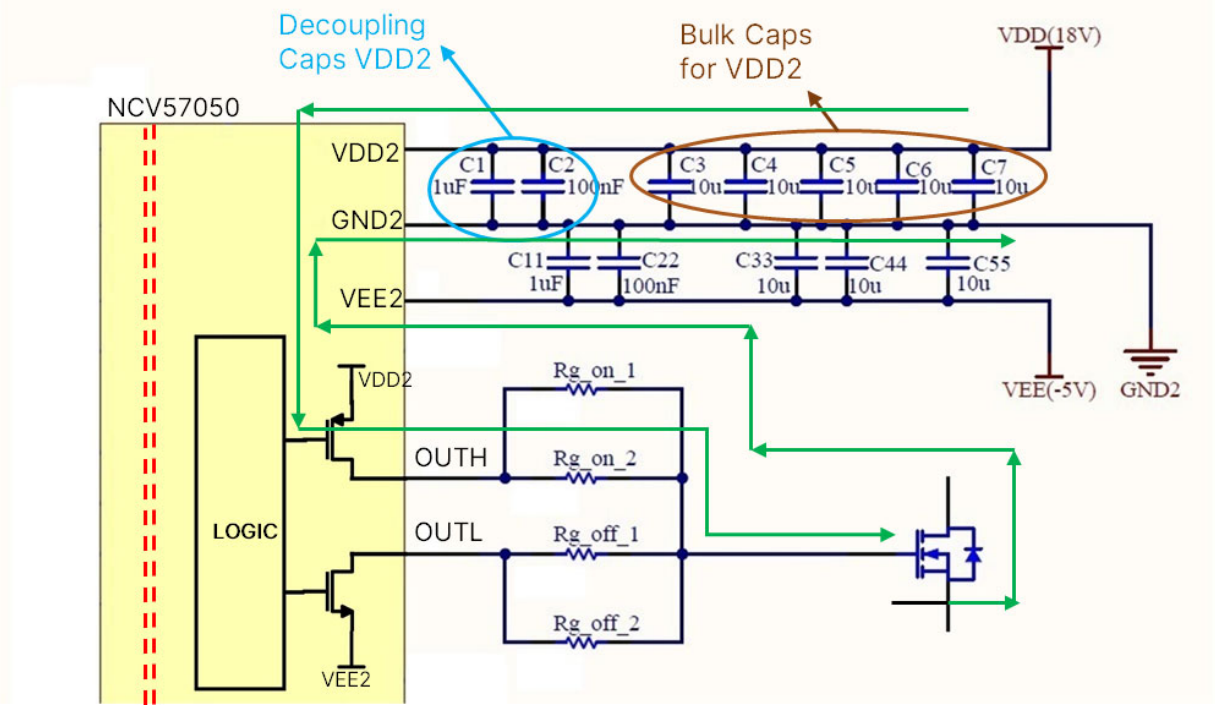

Figure 10. Gate Drive Circuit

The gate current path during turn−on of the MOSFET is highlighted in green in the Figure 10. To achieve best switching performance, it is important to reduce the parasitic inductance in the gate drive path. Since there is no current buffer in the design, it is very important to place the IC NCV57050 as close as possible to the gate and Kelvin source pins of the module. Kelvin source is a dedicated small signal pin which is directly connected to the source of the die, and it is dedicated for control. The turn−on gate current path to the gate of the MOSFET is shown in left side of Figure 11 which includes the VDD2 bulk capacitors, OUTH pin of the IC, R_{gon} and gate pin of the MOSFET. The return path from the Kelvin source pin of the MOSET to GND2 pin is shown on the right side of the Figure 11. The current path to the gate and return path from the source pin should be kept as short as possible to avoid the parasitic inductance. If the two current paths are also placed next to each other, common mode noise on the lines can be reduced too. The gate current loop during turn−off should also be designed similarly.

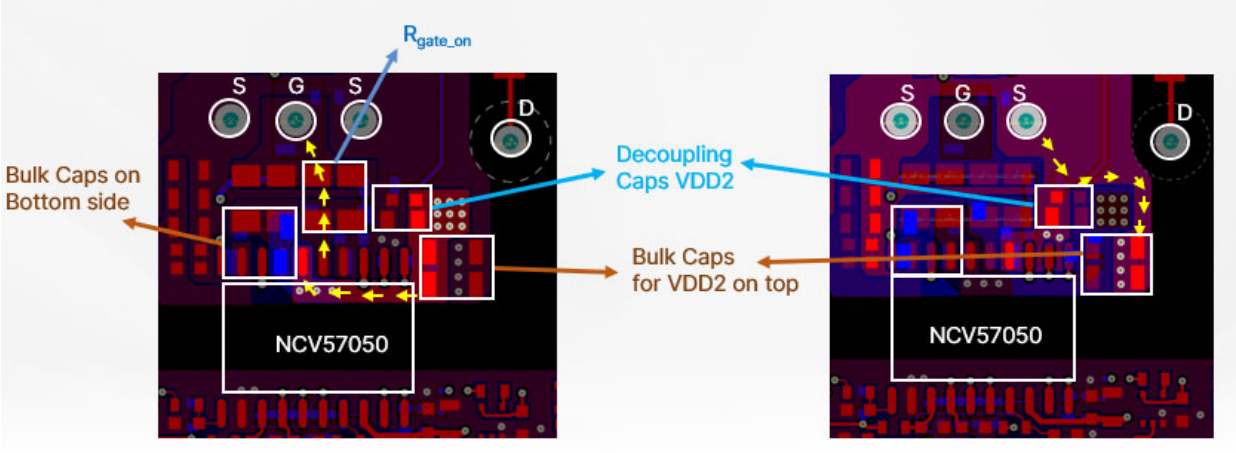

Figure 11. Gate Drive Circuit Layout and Gate Current Path during Turn−on

On the primary side of the IC, it is similarly important to place the decoupling capacitors very close to the VDD1 and GND pins of the IC. As shown in Figure 12, an RC filter can be placed close to the PWM input pins IN+ and IN− of the IC to filter any noise to prevent any unwanted switching.

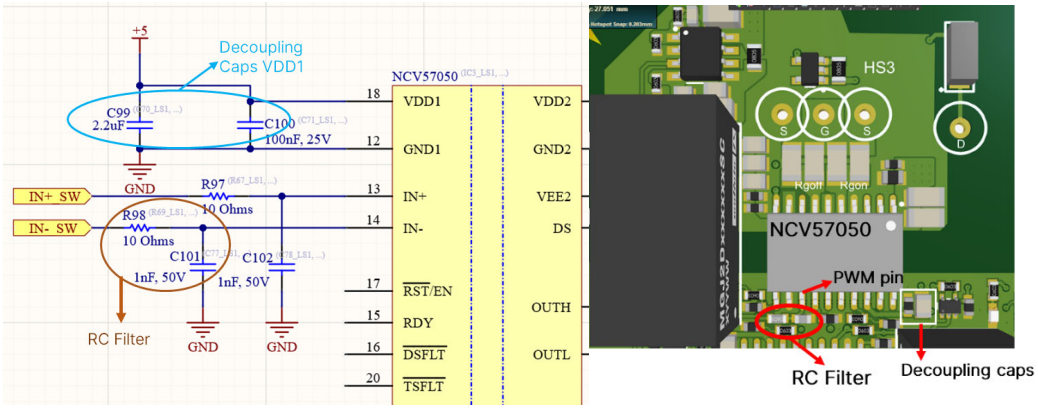

Figure 12. Primary Side Layout of NCV57050

Lastly, as shown in Figure 13, the layout is done symmetrically for all the six switches of the SSDC module to achieve uniform switching performance for all the switches.

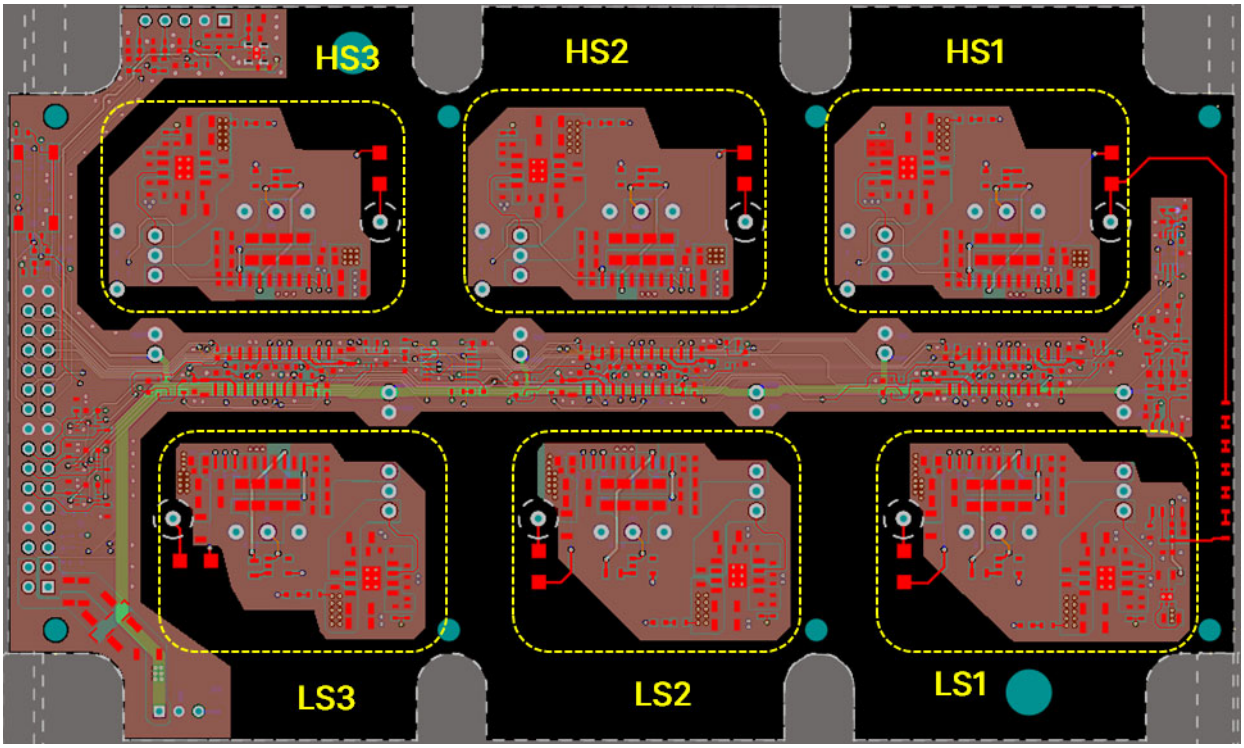

Figure 13. Gate Driver Board Layout

Gate Resistor

The right selection of the correct gate resistor value is a crucial part of the design. The gate resistors have many important functions in a gate driver such as

- The gate resistors control the switching speed of the MOSFET by limiting the peak gate current from the driver, thus directly impacting the losses in the MOSFET during turn on and turn off
- The gate resistors damp the ringing of the gate voltage
- The gate resistors also control the ringing of the drain source voltage of the MOSFET between stray inductance in the commutation loop and the drain source capacitance during turnoff and limit overshoot of the drain source voltage. This ringing impacts the EMI in the system
- The power dissipation that happens in the gate driver IC NCV57050 due to the sink current during turn−off is also limited by the gate resistors

In this design, the gate driver is implemented without current buffer stage, since NCV57050 IC is capable of high sink and source currents. The gate driver circuit including all the internal and external gate resistors is already shown in Figure 9.

The total resistance in the turn−on and turn−off current paths is given by

$$P_{on} = R_{PMOS} + R_{gon} + R_{int} \quad \text{(eq. 2)}$$

$$P_{off} = R_{NMOS} + R_{goff} + R_{int} \quad \text{(eq. 3)}$$

Where, R_{PMOS} is the resistance of the PMOS stage of the gate driver IC NCV57050

R_{gon} is the external turn−on gate resistance

R_{int} is the internal gate resistance of the SiC module

R_{NMOS} is the resistance of the NMOS stage of the gate driver IC NCV57050

R_{goff} is the turn−off gate resistance

This gate driver board is designed for the modules NVXR17S90M2SPB and NVXR22S90M2SPB and tested with these modules. For NVXR17S90M2SPB module, R_{PMOS} = 1 Ω, R_{NMOS} = 1 Ω, and R_{int}= 0.7 Ω. R_{gon}=3.72 Ω and R_{goff}=1.95 Ω are considered in this paper.

Thus, the total turn−on and turn−off resistances are

$$R_{on} = 5.42\ \Omega \quad \text{(eq. 4)}$$

$$R_{off} = 3.65\ \Omega \quad \text{(eq. 5)}$$

The peak current during turn−on and turn−off can be calculated as

$$I_{source\_peak} = \frac{VDD2 - VEE2}{R_{on}} = \frac{18 - (-5)}{5.42} = 4.24\ A \quad \text{(eq. 6)}$$

$$I_{sink\_peak} = \frac{VDD2 - VEE2}{R_{off}} = \frac{18 - (-5)}{3.65} = 6.30\ A \quad \text{(eq. 7)}$$

The peak currents are within the 15 Apk rating of NCV57050.

The selected gate resistor should also have power rating higher than the dissipation in the resistor due to the switching of the MOSFET. The dissipation in the turn−on resistor can be calculated as

$$P_{d\_on} = \frac{1}{2} \times Q_G \times (VDD2 - VEE2) \times F_{SW} \times \frac{R_{gon}}{R_{on}} \quad \text{(eq. 8)}$$

At 16 kHz operation, the P_{d_on} can be calculated as 303 mW. Therefore, considering the derating with respect to temperature, two resistors of 400 mW rating are used in parallel for turn−on resistance as well as turn−off resistance.

Similarly, the dissipation can be calculated for the turn−off resistance.

Active Miller Clamp

Parasitic turn−on of the MOSFET is an unintended turn−on happening due to various reasons. For example, in the Figure 14, when Q1 is turned on, the high dv/dt on the half−bridge node leads to an induced current that charges C_{gs} through the miller capacitance $C_{gd,}$ of complementary MOSFET Q2. This effect induces voltage on the gate of Q2, which when exceeds V_{gs_th} causes parasitic turn−on of Q2. This parasitic turn−on can be prevented by using an Active Miller clamp circuit. Once the voltage on OUTL of Q2 goes below 2 V, the clamp MOSFET is turned on by the gate driver. Then the current induced due to high dv/dt can be redirected to the negative voltage rail (VEE) through a low−impedance CLAMP MOSFET,

thereby preventing the parasitic turn−on. For NCV57050, the clamp MOSFET is not included in the driver package, so it must be externally provided by the user.

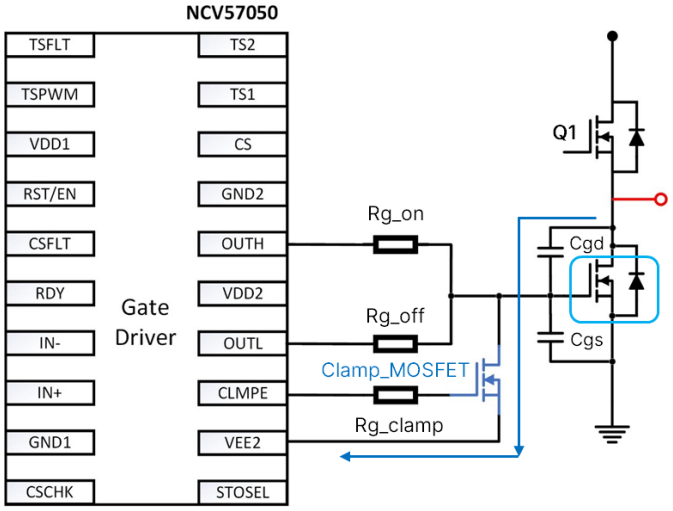

Figure 14. Active Miller Clamp Circuit

Protection

NCV57050 Protection Features

NCV57050 has three different fault monitoring features as shown in Figure 15. All the features result in an active low output on their respective pins when there is a fault. The three fault outputs are as follows:

RDY – active low when UVLO protection for VDD1, VDD2 or TSD (temperature sense of NCV57050) is triggered

TSFLT – active low when module encounters high temperature condition (NTC)

DSFLT – active low output when short circuit occurs (DESAT circuit)

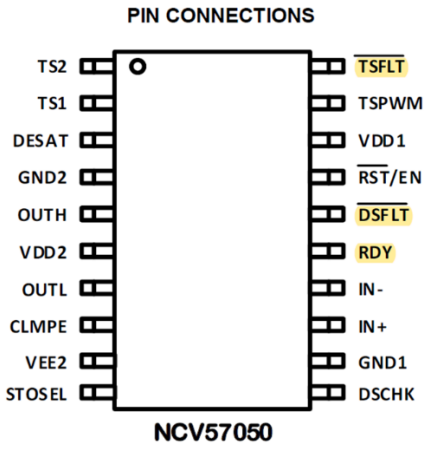

Figure 15. Fault Monitoring of NCV57050

Short Circuit Protection

DESAT circuit is used to detect short−circuit in IGBT application, which can also be used with SiC devices with slight modifications. Before understanding how the DESAT circuit works, it is important to know the differences between IGBT and SiC at short circuit condition, as shown in Figure 16. During short circuit condition, IGBT which is normally operating in saturation region, moves to active region as the collector current I_c increases sharply. The I_c gets self−limited and becomes independent of V_{ce} and hence the power dissipation also becomes self−limited. On the other hand, SiC MOSFET works mostly in the linear region even during short−circuit condition, which results in a very high saturation current. This effect combined with the smaller die size of SiC, the short−circuit withstand time of SiC is typically between 1 to 3 μs, whereas IGBTs have a withstand time of 5 μs typically.

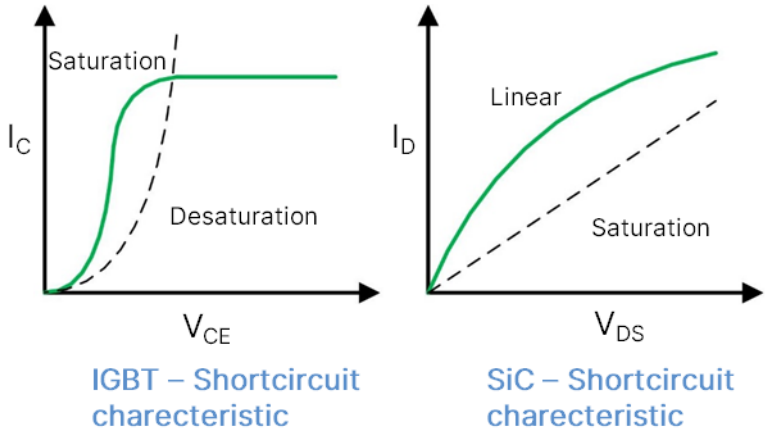

Figure 16. Short Circuit Characteristics of IGBT and MOSFET

During short circuit in SiC, the current I_c continues to rapidly increase, which causes an increase in V_{DS}. DESAT circuit detects the short−circuit indirectly by detecting the increase in V_{DS}. The DESAT circuit is shown in Figure 17. During normal operation and when the SiC is in ON state, VDD2 charges the blanking capacitor C_B and the V_{CB} is clamped to the forward voltage of the D_{DESAT}. As already discussed, during short circuit I_C increases and thus V_{DS} increases and V_{CB} continues to further charge. Once the voltage on the DESAT pin or the V_{CB} increases beyond V_{DESAT_THR}, the comparator creates a DESAT Fault, detecting a short−circuit. NCV57050 is designed to internally shut−down the gate signals if the short−circuit is detected.

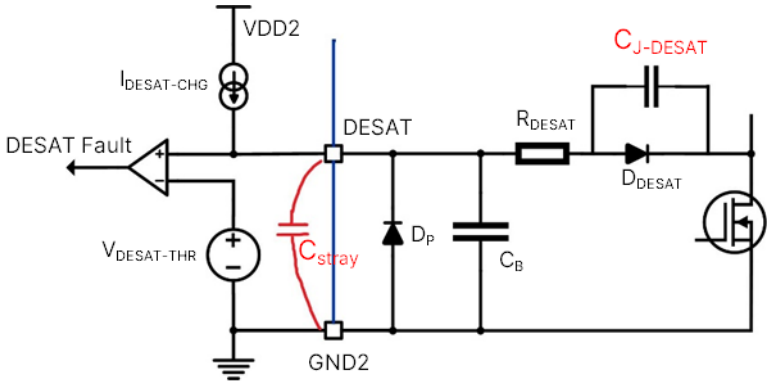

Figure 17. DESAT Circuit for Short−circuit Detection

The main function of the capacitor C_B is to create a blanking time. Blanking time is the delay between the turn−on signal for the MOSFET and the point at which the short−circuit is detected. One should choose the blanking time carefully, so that the blanking time is:

1. Long enough to prevent false detection of short circuit
2. Short enough to shut−down the device before damage

Typical blanking time of DESAT circuit for SiC applications is less than 2 μs. The equation for the blanking time is given as

$$t_{BLANK} = t_{LEB} + \frac{C_B \times (V_{DESAT-THR} - V_{D-OFFSET})}{I_{DESAT-CHG}} \quad \text{(eq. 9)}$$

And the voltage at which the short circuit is detected is given by the equation:

$$V_{DESAT-TRIP} = V_{DESAT-THR} - (I_{DESAT-CHG} \times R_{DESAT}) - V_{F-DESAT} \quad \text{(eq. 10)}$$

Once the short−circuit is detected by the DESAT circuit, a hard turn−off of the MOSFET will leads to V_{DS} overshoot and over−voltage stress. For this reason, a soft turn−off is required. This can be achieved by the STOSEL pin as shown in Figure 18. Soft turn−off facilitates the discharge of the MOSFET gate with smaller currents through the STOSEL pin. This is achieved by using R_{g_stosel} value much larger than the normal R_{g_off}. Thus, the device turns off at a much slower rate reducing the voltage overshoot and therby preventing damage to the motor windings.

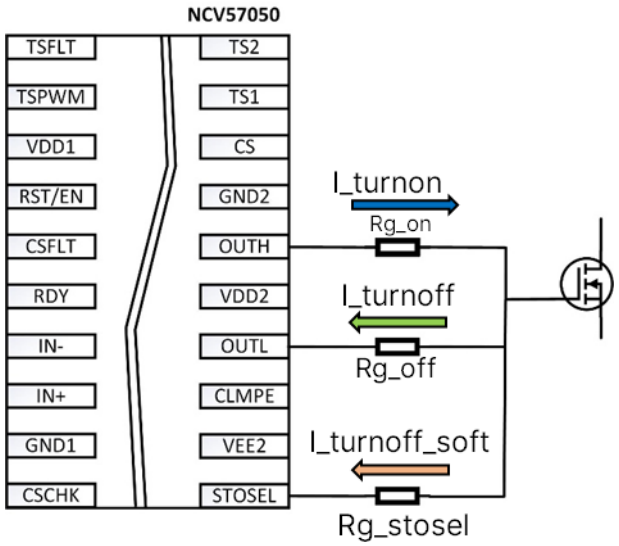

Figure 18. SOFT Turn−off Function

Temperature Monitoring

NCV57050 has two isolated measurement channels for temperature measurement. The TSPWM pin outputs the module temperature measurement in the form of a 10 kHz pwm output. The duty cycle increases with temperature. The pwm measurement can be converted to a simple analog measurement output by adding an RC circuit as shown in Figure 19.

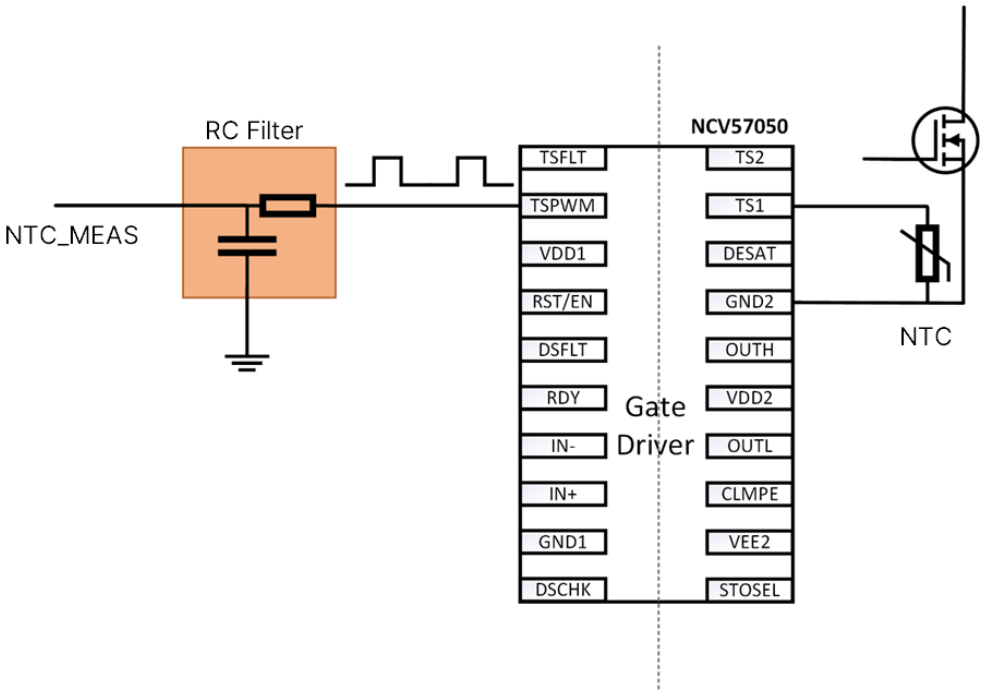

Figure 19. NTC Temperature Measurement

DC Link Monitoring

The dc link voltage is measured, which might be needed for the control of the traction inverter and also for protection of the system in case of over−voltage conditions. The dc link voltage is measured using an external circuit, as shown in the Figure 20. The dc link voltage is connected to a voltage divider, and this is provided as an input to an isolation amplifier. The isolation amplifier isolates the measurement from the high voltage ground and converts single ended measurement to differential measurement. The differential measurement can also be converted to single ended depending on the requirement.

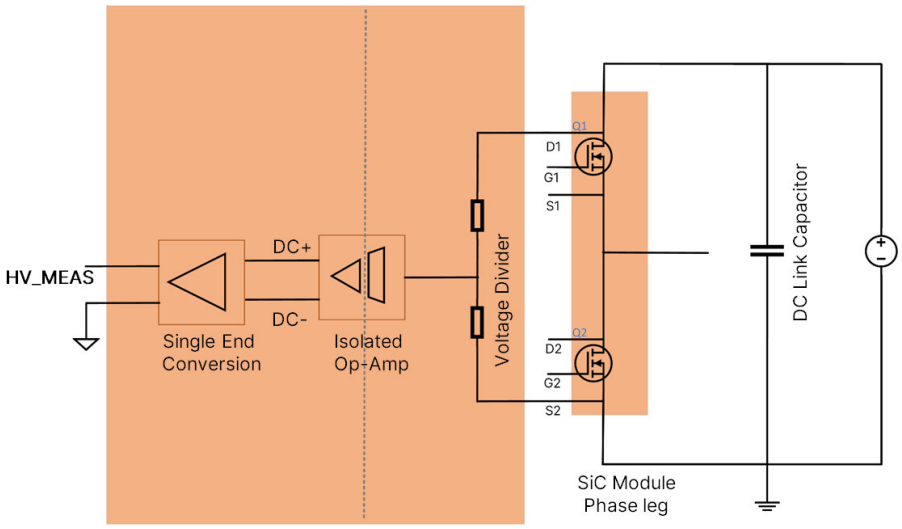

Figure 20. DC Link Voltage Measurement

Overall Protection Scheme

On the gate driver board, all the various protection and monitoring features are lumped together. All the faults are processed through OR gates as shown in Figure 21. The NCV57050 generated faults are shown in blue. The remaining two faults are triggered when the dc link monitoring detects an over voltage or if the gate driver under voltage protection is detected. Once any of these faults occur, the fault is latched and the PWM signals are turned off with a programmable delay.

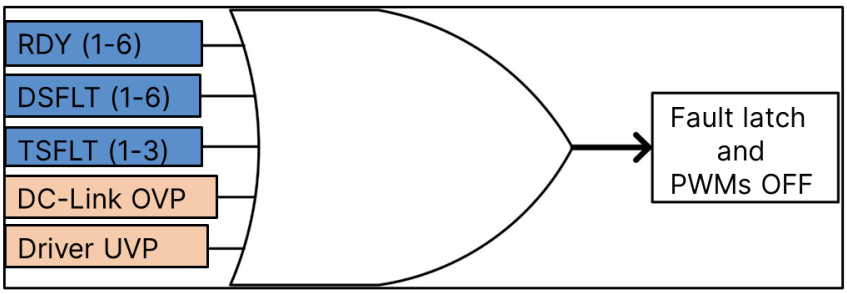

Figure 21. Fault Logic on Gate Driver Board

Power Up Sequence

During the powering up of the gate driver board, it is crucial to ensure safe power up of the gate driver. Operating the inverter should be avoided till all the required voltages have reached the final values. Also, in case there is a fault on the board during powering up, then the switching and operation of the inverter should be avoided. Therefore, a safe power up scheme is implemented as shown in Figure 22. On power−up of the board, all the PWMs are disabled by the latch circuit which is in High state by default.

When there is no fault at startup:

When VDD1, VDD2 and VEE2 reach the required voltage, and if there are no faults in the system, the fault signal goes to low state. Now the LATCH can be cleared using the software or by pressing the RESET switch on the gate driver board. At this point the PWMs are enabled, and the inverter is ready for operation.

When there is a fault at startup:

Then, everything should be powered off and the fault should be debugged before turning on the inverter again.

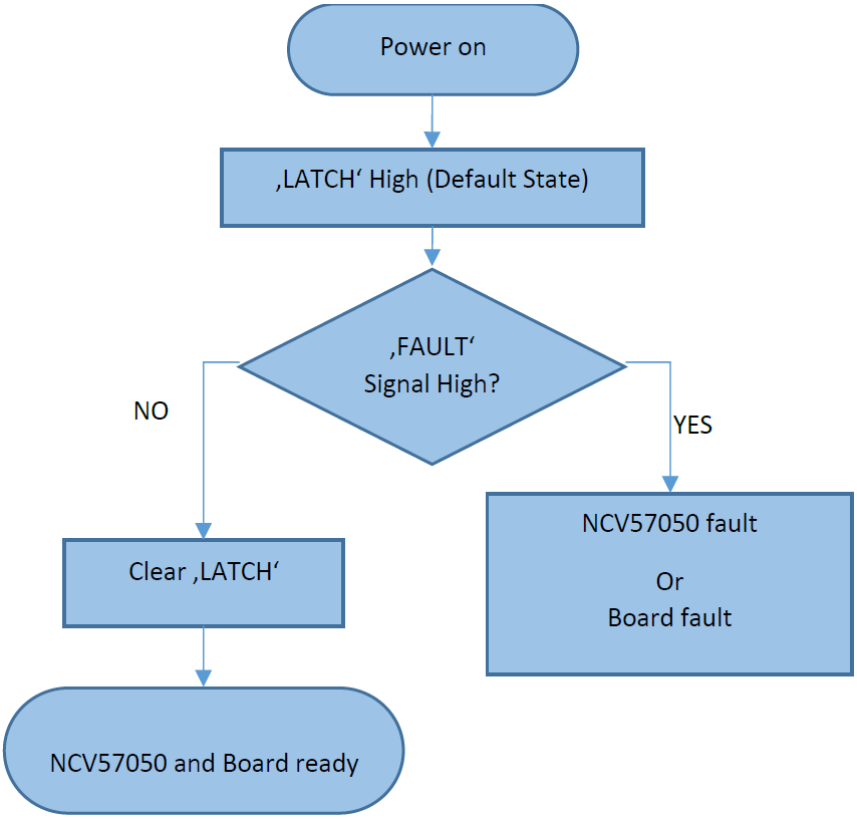

Figure 22. Power Up Sequence

Test Results

Double Pulse Test (DPT)

A DPT is used to analyze the switching behavior of the MOSFET and to calculate the switching energies during turn−on, turn−off, and the reverse recovery process. In DPT, one of the switches of a half−bridge is held in off state by having a constant negative bias voltage on the gate and the other switch (DUT) is tested with 2 gate pulses and a Load inductor, as shown in Figure 23. In the next section, low−side MOSFET is considered as DUT. When the low−side MOSFET(DUT) is turned on, the current flows through the load inductor and through the DUT. When the DUT is turned off, the current freewheels through the body diode of the upper switch.

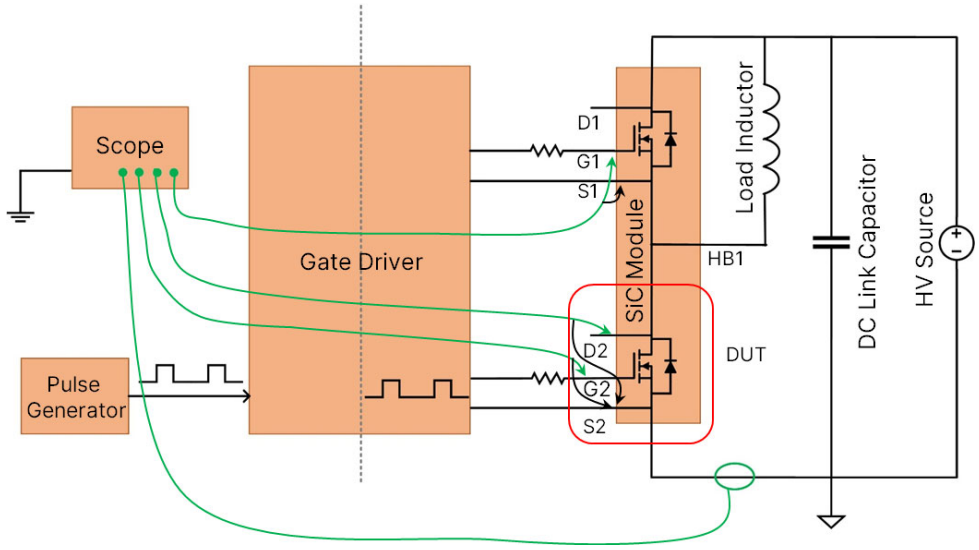

Figure 23. Power Up Sequence

Test Setup

The test is conducted on the low side switch of the half−bridge. The test circuit is already shown in Figure 23. And a picture of the test setup is shown in Figure 24. The test setup used is as follows:

- SiC power module: ENGNVX90VR02WSTB(8D)
- DC link capacitor: SBE 700A50795−186, 500 μF 500 V
- Gate source voltage measurement: Lecroy HVD3106 (120 MHz)
- Drain source voltage measurement: Pico TA042 (100 MHz)
- Drain current measurement: Rogowski PEM CWTUM/6/R (30 MHz)

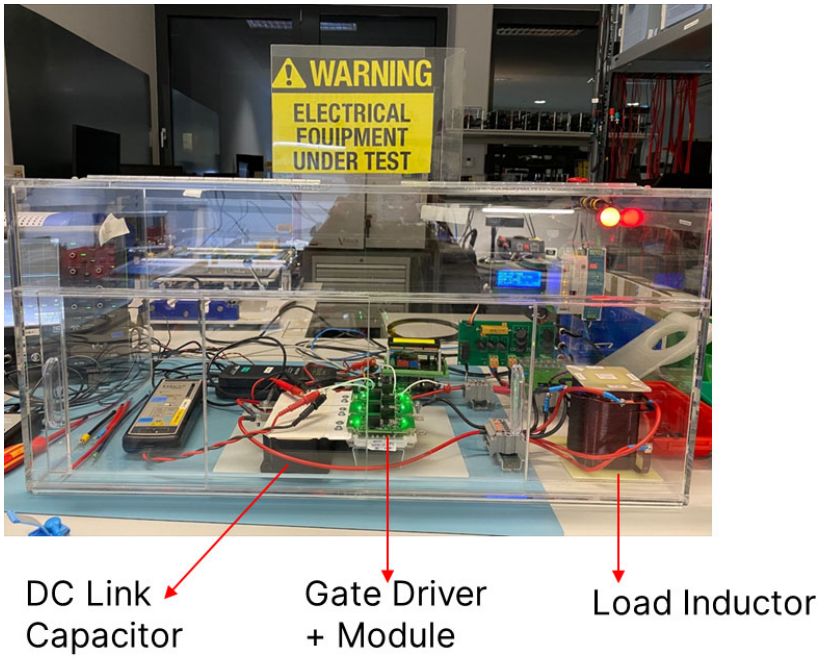

Figure 24. DPT Test Setup

Test Conditions

Table 2. TEST CONDITIONS FOR TURN−ON

Parameters	Value
V_{dc}	435 V
I_{drain}	900 A
T_{amb}	25°C
L_{load}	10 μH
R_{gon}	3.72 Ω
R_{goff}	1.95 Ω

Test Results

Turn−on

The waveforms during the turn−on process of the MOSFET are shown in Figure 25.

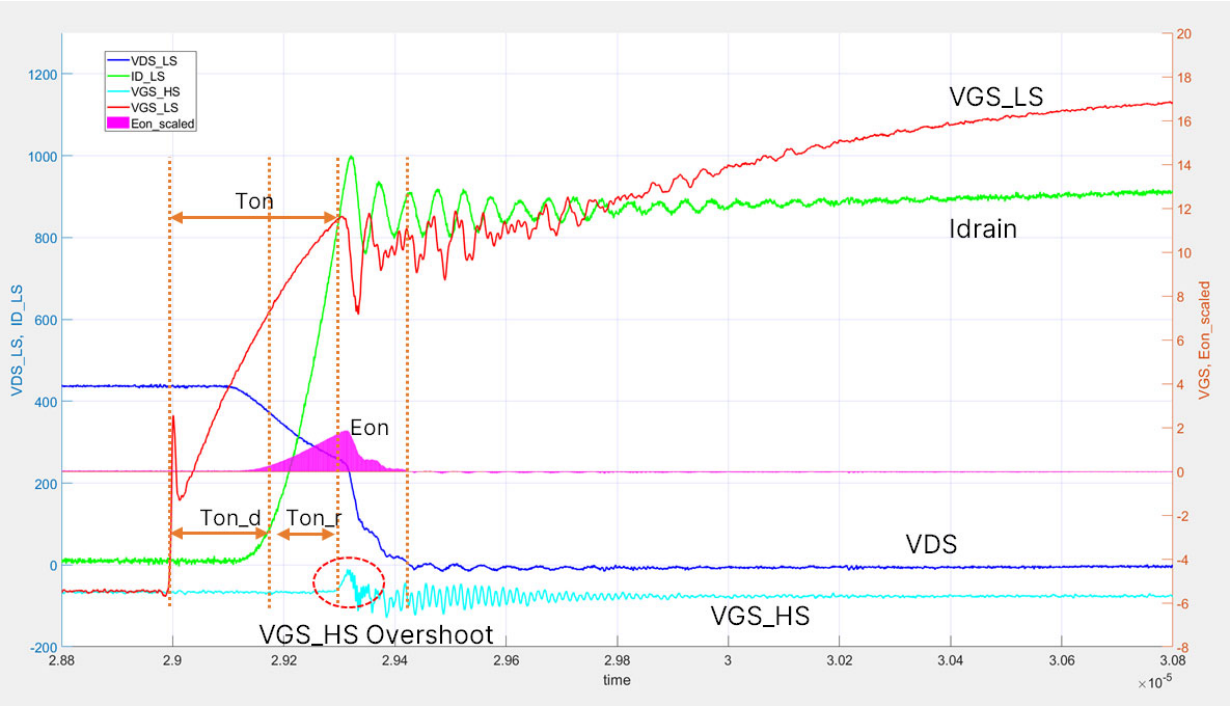

Figure 25. Turn−on Waveform

Table 3. TEST RESULTS FOR TURN−ON LOSS

Parameters	Value
T_{on_delay}	179 ns
T_{on_rise}	119 ns
T_{on}	287 ns
E_{on}	26.8 mJ
dI/dt	6.05 A/ns (10% to 90%)
dI/dt	−4.46 V < V_{th}

As can be seen, the gate driver turns on the SiC safely. The gate voltages and the drain current ringing are within acceptable range. The gate source voltage (V_{GS_HS}) of the complementary switch of the half−bridge (high−side switch) is held low by the active miller clamp circuit which ensures that it stays well below the gate threshold voltage V_{th} , thus avoiding Parasitic turn−on (PTO) condition. Lastly, the turn−on energy E_{on} from the test is close to the value in the datasheet of the module.

Turn−off

The waveforms during turn−off of the switch are shown in Figure 26.

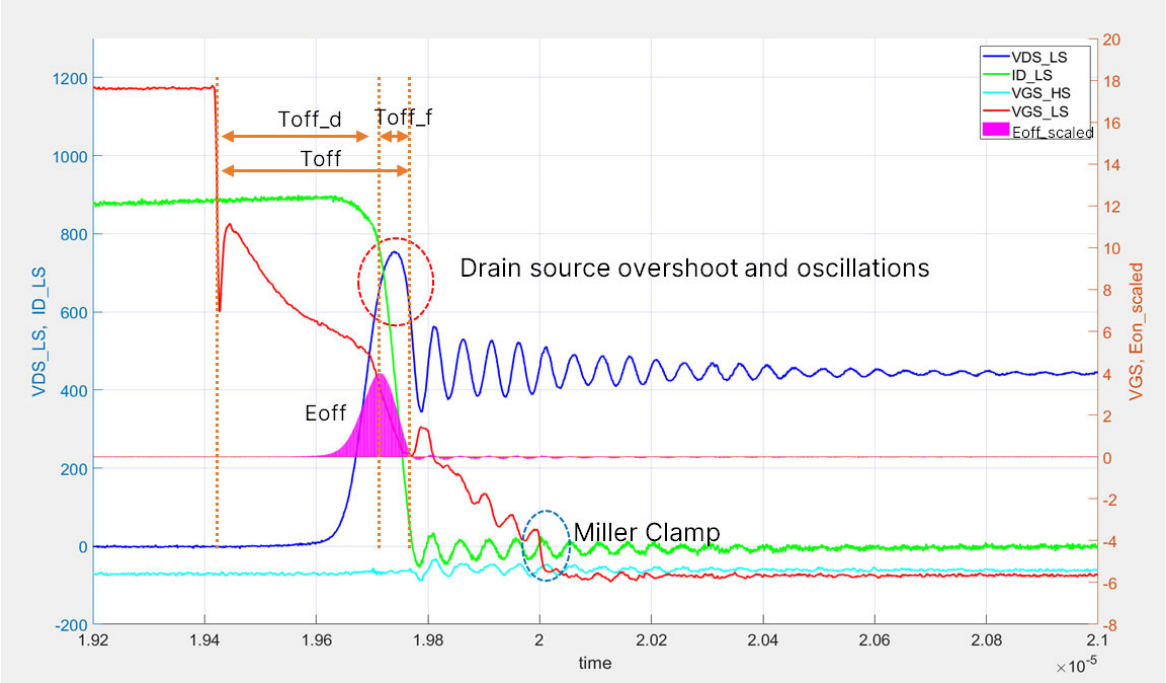

Figure 26. Turn−off Waveform

Table 4. TEST RESULTS FOR TURN−OFF LOSS

Parameters	Value
T_{off_delay}	285 ns
T_{off_fall}	59 ns
T_{off}	344 ns
E_{off}	37.1 mJ
dV/dt	10.9 V/ns (55% to 85%)
V_{DS_peak}	−756 V < V_{DS_max}

During the turn−off process, there is an overshoot and oscillations of the drain source voltage. As can be seen, the overshoot is kept below the V_{DS} rating 900 V of the module. The oscillations of the drain source voltage and the gate source voltage are acceptable. The undershoot of the complementary switch gate source voltage is also limited by the active miller clamp thus there is no damage to the switch. Therefore, it can be concluded that the gate driver is able to turn off the SiC safely.

SC Test

Short circuit tests are generally conducted to determine a safe operating area for MOSFET. Short−Circuit test can be done by three test methods.

Test Setup

In this work, the Short−circuit test is done on the low side switch(Q2) of half bridge, with type 1 method as shown in Figure 27.

- SiC power module: ENGNVX90VR02WSTB(8D)
- DC link capacitor: SBE 700A50795−186, 500 μF 500 V
- Gate source voltage measurement: Lecroy HVD3106 (120 MHz)
- Drain source voltage measurement: Pico TA042 (100 MHz)
- Drain current measurement: Rogowski PEM CWTUM/6/R (30 MHz)

Test Condition

As shown in Figure 27. Device Q1 is always kept on and V_{GS_HS} value is set greater than 15 V in order to make Q1 saturation current larger than Q2 saturation current.

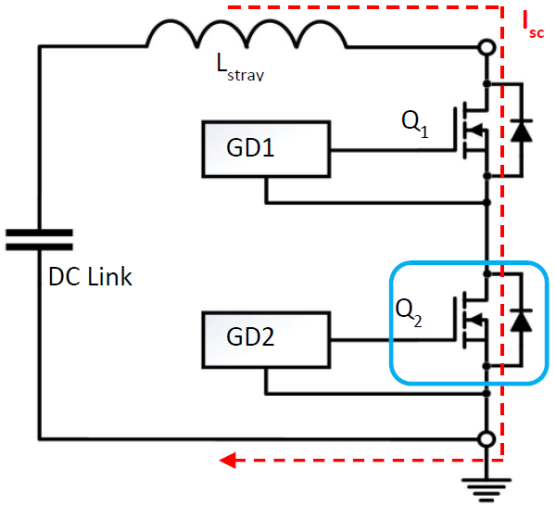

Figure 27. Type 1 Short Circuit Test

Under on−state of Q1, Q2 is turned on by applying a gate pulse of 6 μs (V_{GS_LS}). Then the short circuit current is measured as shown in Figure 28. DESAT function of high side switch gate driver is turned off during this period of time, so that the upper MOSFET doesn't turn−off during the test due to DESAT/short−circuit fault.

Table 5. SHORT CIRCUIT TEST OPERATING POINT

Parameters	Value
DC link voltage	450 V
Pulse applied	6 μs
T_{amb} = 25°C	25°C
Short circuit current	~ 10.6 kA peak

Test Results

SiC power module has lower short circuit withstand time as compared to IGBT because of smaller die size. SiC has larger linear region and due to which it cannot self−limit I_{SC} which keeps ramping up, which further leads to increase in $V_{DS.}$ On other hand for IGBT, I_{SC} remains constant in active region. In SiC MOSFET as I_{SC} affects V_{DS}, DESAT measures V_{DS} which indirectly measures I_{SC}. Blanking time should be long enough to prevent false trip but short enough to shut down before the damage of the device. As shown in Figure 28, the Blanking time is 2.06 μs and short circuit withstand time (SCWT) is 2.67 μs. Short circuit energy (E_{sc}) is dependent on the size of the DC−link capacitor. Energy loss during this short circuit test is 12 J which is also represented in Figure 29.

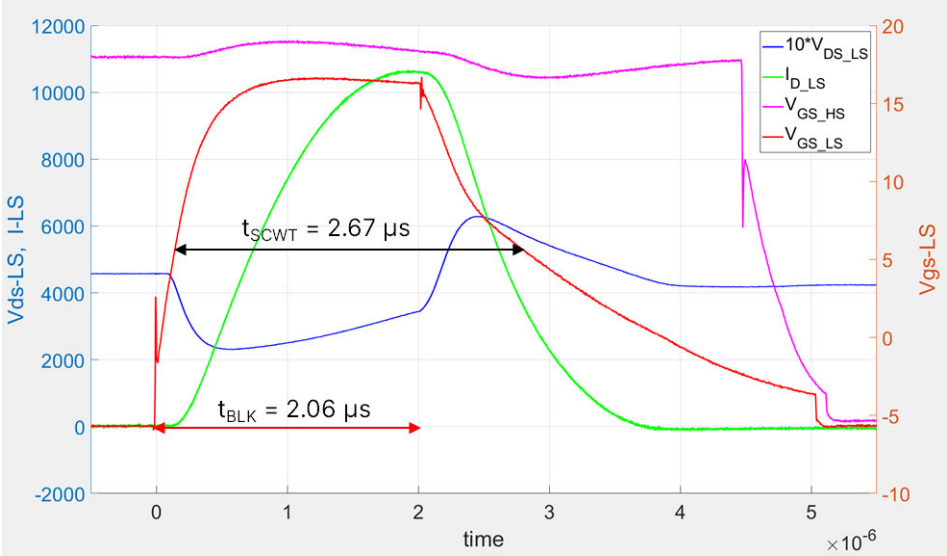

Figure 28. Short Circuit Test Waveform

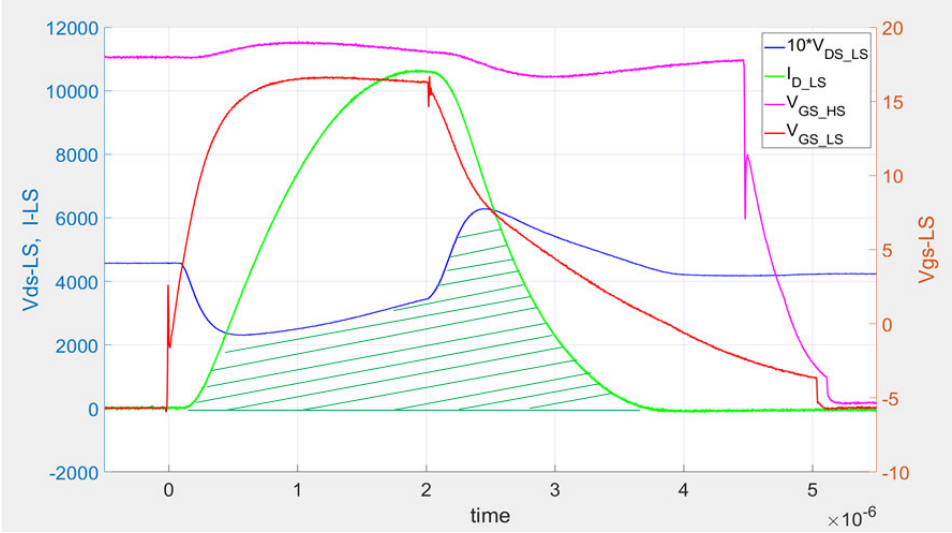

Figure 29. Energy Loss during Short Circuit Test

Inductive Load System Test

Single−phase Test

Load test of a single half−bridge of the inverter is required to make sure that the gate driver board is functional at full load condition. If the results of this test are successful, there is a good possibility that the remaining two half bridges are also fully functional, because the schematics and the PCB layout of all three half bridges are very identical. One more advantage of having a single−phase test setup instead of a three−phase setup is the requirement of space and infrastructure is relatively less. The single−phase test circuit is shown in Figure 30 and the test setup is shown in Figure 31. The SSDC gate driver is connected to the module and the module is connected to the DC link capacitor C1. The half bridge point is connected to the load inductor L1. The other end of the inductor is connected to a capacitive voltage divider formed with C1 and C2. The inductor L1 is an air−core inductor, and the capacitor bank is a PCB designed with film capacitors. When sinusoidal pulse width modulation scheme (SPWM) is used, a resulting sinusoidal current can be measured on the inductor as shown in Figure 32. By increasing the modulation index, the resulting phase current can also be increased. Since there is no resistive load or mechanical load connected in the circuit, the phase current is recycled and hence, the power supply only needs to compensate for the losses in the system.

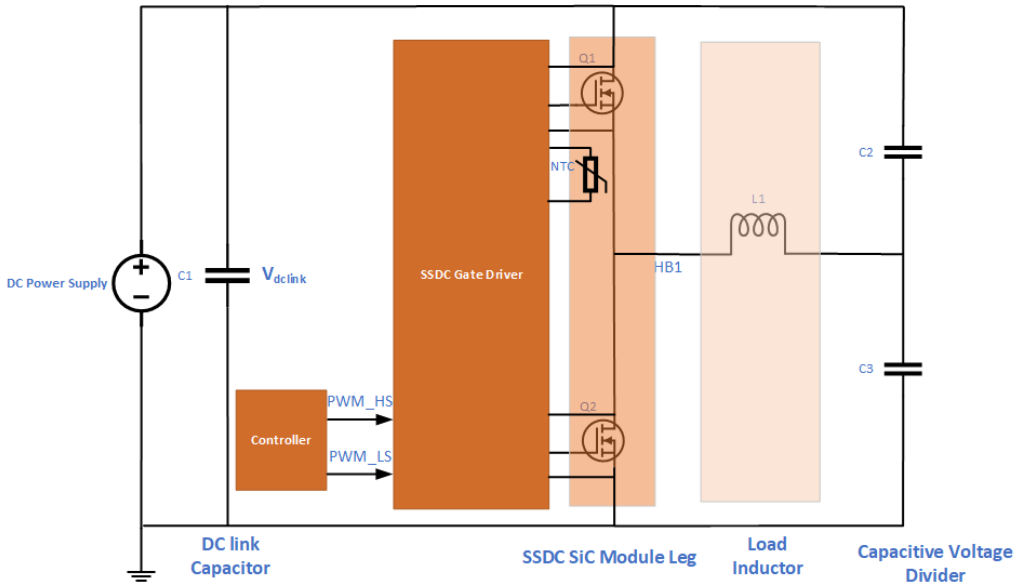

Figure 30. Single Phase Load Test Circuit

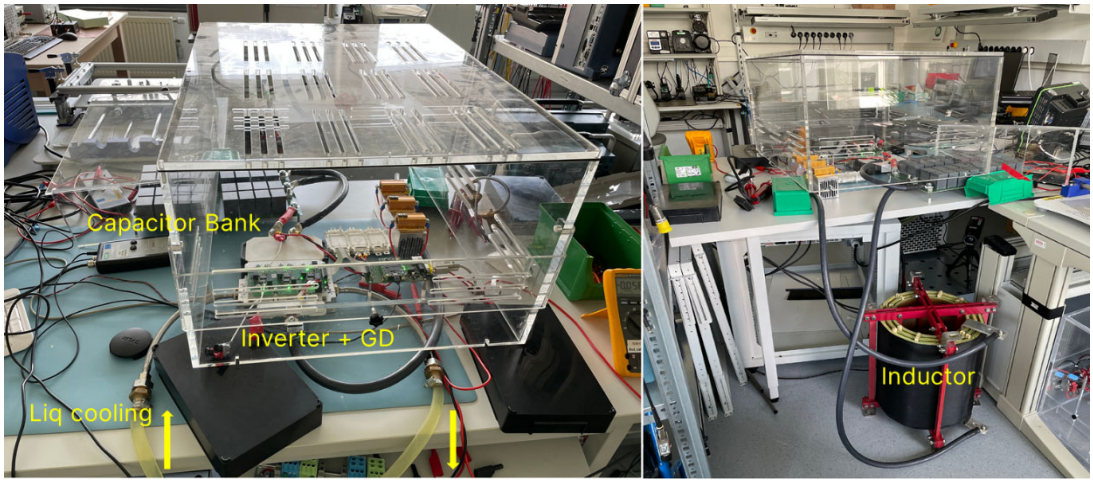

Figure 31. Single Phase Load Test Setup

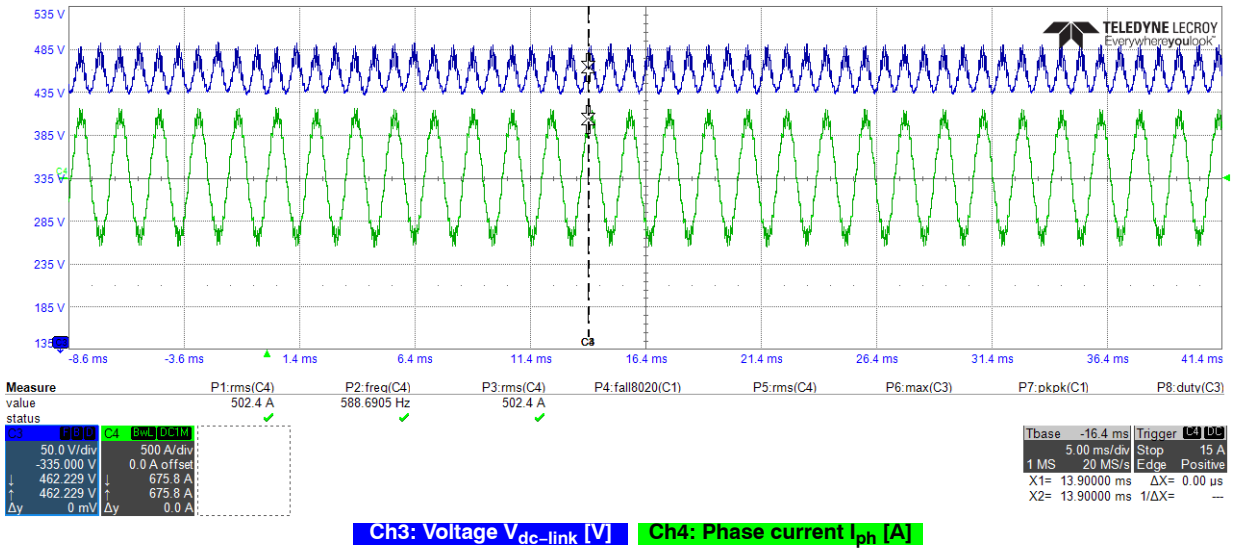

Figure 32. Waveforms of Phase Current and DC Link Voltage

Table 6. SPECIFICATIONS OF THE SINGLE−PHASE TEST

Parameter	Value
V_{dc}	450 V
I_{ph}	500 A rms
f_{ac}	580 Hz
L1	65 µH
C1, C2	320 µF
Ambient temp	25°C
Ambient temp Chiller	25°C
Time span	10 mins

Observations:

The load testing with phase current of 500 A rms at a Vdc of 450 V, is done for 10 minutes and the corresponding waveforms are shown in Figure 32. The gate driver board and all other parts of the test circuit endured the testing successfully. The chiller temperature increased from ambient temperature of 25°C to max of 38°C after the test and the module temperature recorded from the integrated NTC is 30°C. Maximum temperature recorded on the inductor is 70°C. Care should be taken to avoid any metallic objects in the vicinity of the air conductor, as eddy currents induced in the metal objects may result in dangers. These eddy current will also contribute to higher power consumption from the dc power supply. As mentioned, although the energy in this circuit is recycled, due to the resistive elements in the inductor, wires and capacitors, the dc supply must still provide for the losses, which in this test was approximately 3 kW of losses for a power test of 48.13 kVA.

Three−phase Test

For this test, the inverter is connected to inductive load as shown in Figure 33. The test circuit is similar to the single−phase test, each half−bridge point is connected to each load inductor, and the other side of the load inductors is connected together to form a star point. The same air core inductor used for single−phase test is used for this test, and the capacitor bank is not needed anymore to generate a sinusoidal current. SPWM is used to generate sinusoidal phase currents. The test setup is shown in the Figure 34. Three−phase circuit has a wider operational range compared to the single−phase setup. In case of single−phase test, the size of the capacitor bank required for generating sinusoidal phase current at lower frequencies is significantly large, while in the three−phase test, the capacitor bank is not needed at all.

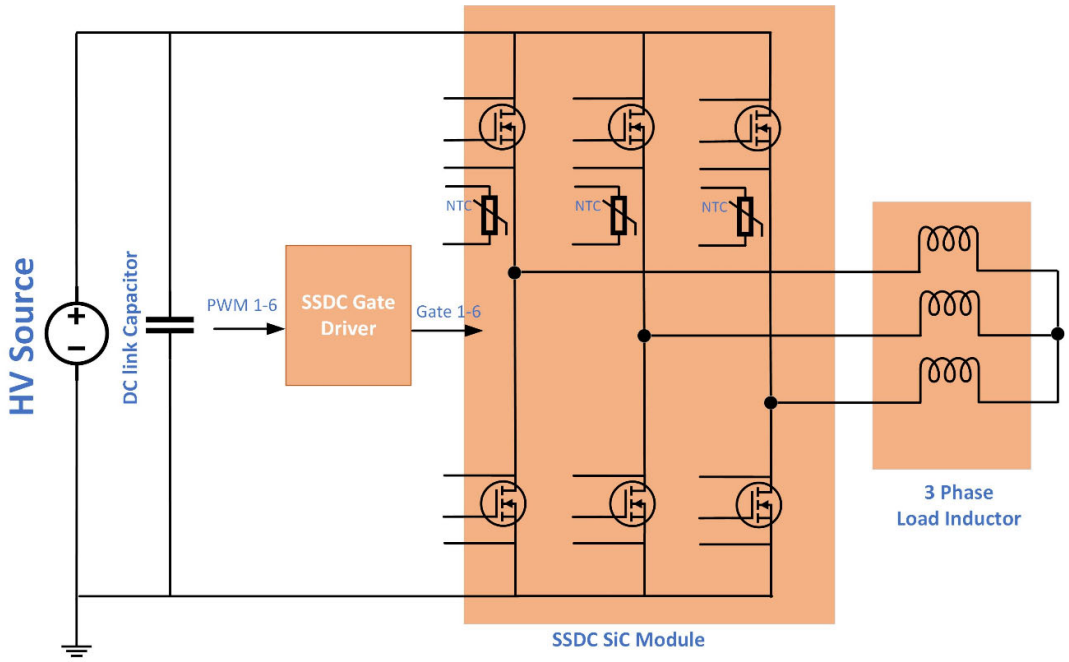

Figure 33. Three Phase Load Test Circuit

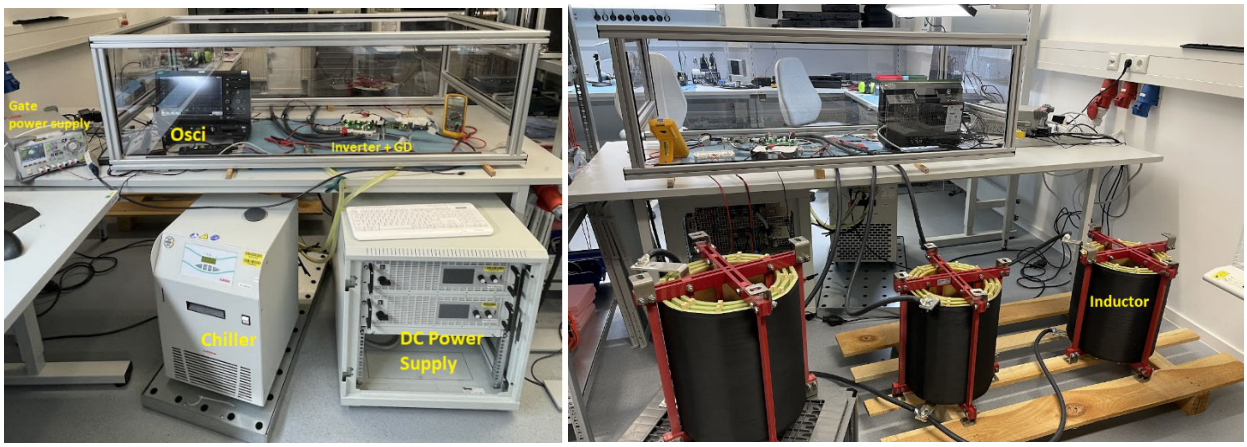

Figure 34. Three−Phase Load Test Setup

Table 7. SPECIFICATIONS OF THE THREE−PHASE TEST

Parameter	Value
V_{dc}	420 V
I_{ph}	500 A rms
f_{ac}	580 Hz
L1, L2, L3	65 μH
C1, C2	320 μF
Ambient temp	25°C
Ambient temp Chiller	25°C
Time span	6 mins

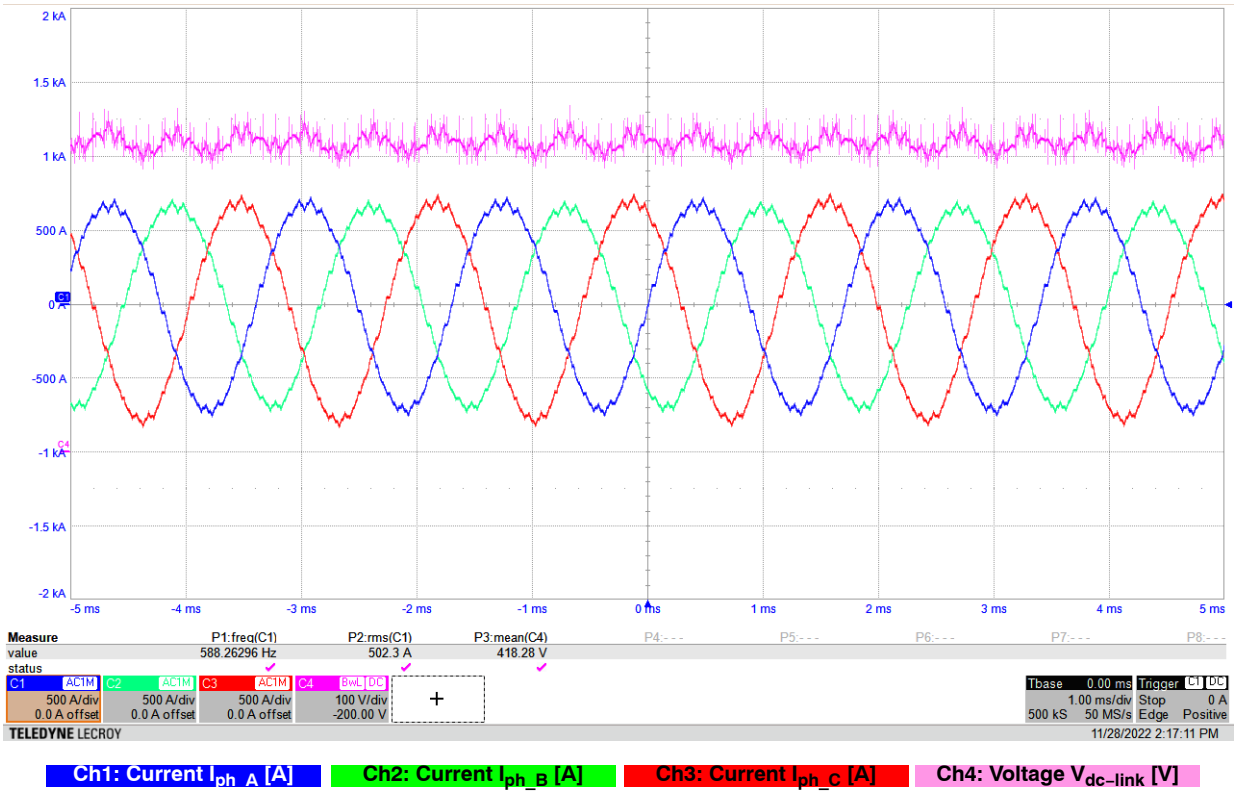

Figure 35. Waveforms of Three−phase Load Test

Observations:

The load testing with a phase current of 500 A rms at a Vdc of 420 V, is done for 6 minutes and the corresponding waveforms are shown in Figure 35. The gate driver board and all other parts of the circuit endured the testing successfully. The chiller temperature increased from ambient temperature of 25°C to max of 65°C after the test and the module temperature recorded from the integrated NTC increased from 25°C to 45°C. Maximum temperature recorded on the inductor is 77°C. The power required from the dc power supply is approximately 7.8 kW for a power test with apparent power of 170 kVA through SiC module. Because of the inductive load, most of the power is reactive.

Summary

Gate driver design is very crucial to achieve high efficiencies and safety requirements for traction applications. As the gate drivers in the market tend to get smarter, its challenging to use all the features provided by the driver in a reliable way while keeping the system level design simple. This work provides a good introduction on how the NCV57050 features work and also on the design steps required to realize a traction inverter application.

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