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Understanding Loop Compensation with Monolithic Switchers

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Introduction

Monolithic switchers, such as members of the NCP101X or the NCP1027 series, associate a current-mode controller and a power MOSFET on a single-die construction. Unlike traditional solutions implementing an external sensing resistor, these switchers embed everything inside the package and can sometimes puzzle the power supply designer looking for a familiar configuration. This application note details what is inside these switchers and will guide you on how to stabilize them using proven compensation techniques.

Sensing the Inductor Current

All members of the NCP101X and NCP1027 series implement the fixed-frequency peak current mode control technique. This technique implies the cycle-by-cycle sensing of the inductor current, its peak being controlled by the feedback loop. The current information is usually conveyed to the controller via a sensing element, the sense resistor. Figure 1 represents a simplified view of a current-mode controller using an external sense resistor:

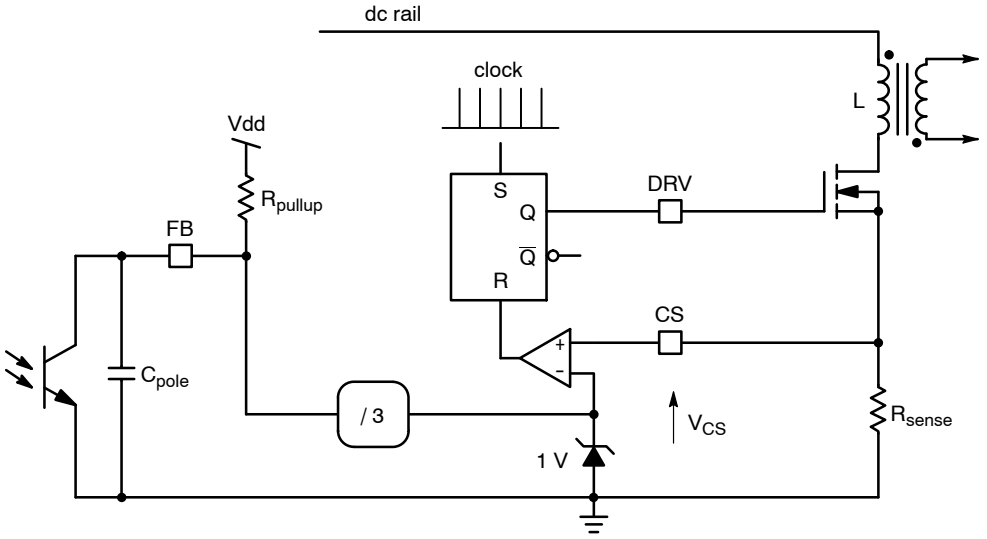

Figure 1. An External Sense Resistor Monitors the Current Circulating in the Primary Inductor of this Flyback Power Supply

The clock initiates a switching cycle by turning the MOSFET on. The inductor current builds-up until it reaches a level imposed by the feedback loop via the internal divider by 3. At this point of time, the current sense comparator trips and turns the MOSFET off until a new clock cycle occurs. By adjusting the feedback level, the control loop has a means to set the inductor peak current to cope with the input / output operating conditions. A kind of active zener diode makes sure the maximum voltage excursion across the sense resistor cannot exceed a certain voltage in case the loop is open. This happens during the startup sequence (until the output reaches the target) or in short-circuit conditions. In the vast majority of controllers, i.e. the NCP1200 series, this voltage is clamped to 1 V. In that case, the maximum inductor current I_L is limited to:

$$I_{L,peak} = \frac{V_{CS}}{R_{sense}} \qquad \text{(eq. 1)}$$

The internal divider by 3 increases the voltage excursion on the optocoupler collector up to 3 V to offer a better dynamics on the feedback pin while also improving the converter noise immunity.

The Need for Internal Sensing

In a monolithic switcher, there is no external sense resistor. Why? First because the proprietary ON Semiconductor Very High Voltage Integrated Circuit (VHVIC) technology does not lend itself to the classical positive current sensing technique as it appears on Figure 1. Second, integration pushes the semiconductor vendors to pack more elements inside the silicon die. The sense resistor was a natural candidate for this move and is now part of the controller. However, we are not exactly dealing with a sense resistor. The retained technique is called Kelvin sensing. A specific cell is added to the power MOSFET and "steals" away a small portion of the drain current at no power dissipation expenses. Ref. [1] describes the technique for discrete components. In a NCP101X switcher, the internal schematic for the feedback section appears in Figure 2. We can clearly see a similar configuration except that the equivalent sense resistor is extremely small (178 mΩ) and thus requires an internal voltage limit of 80 mV. For this particular version, the NCP1014, the maximum peak current is limited to:

$$I_{L,peak} = \frac{80\ m}{178\ m} = 450\ mA \qquad \text{(eq. 2)}$$

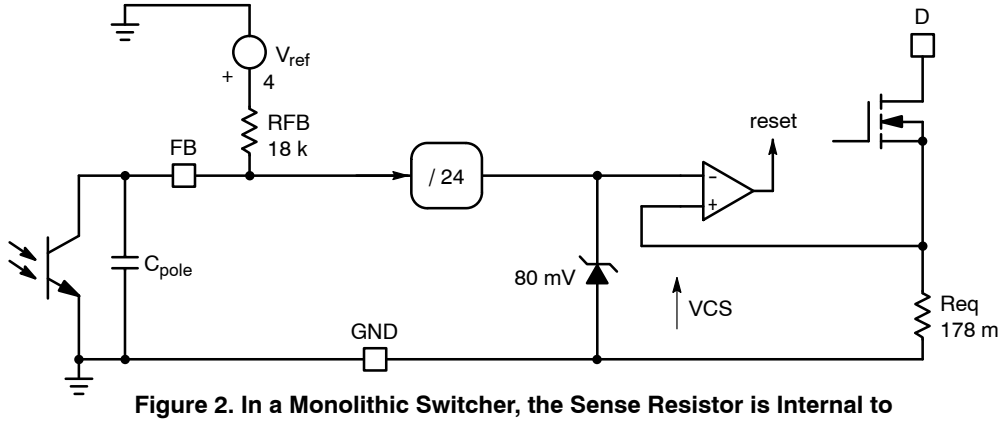

Figure 2. In a Monolithic Switcher, the Sense Resistor is Internal to the Device. Here, an Example with the NCP101X Series

For other switcher versions within the 101X family, the internal equivalent sense resistor changes. We will have:

Device	Peak Current	Equivalent Sense Resistor
NCP1014	450 mA	178 mΩ
NCP1013	350 mA	228 mΩ
NCP1011/12	250 mA	320 mΩ
NCP1010	100 mA	800 mΩ

The NCP1027 series slightly differs in terms of implementation but the idea remains the same. Figure 3 portrays the simplified internal circuitry of this recent switcher where the internal equivalent sense resistor reaches 387 mΩ. In this particular case, the maximum peak current is given by:

$$I_{L,peak} = \frac{310\ m}{387\ m} = 800\ mA \qquad \text{(eq. 3)}$$

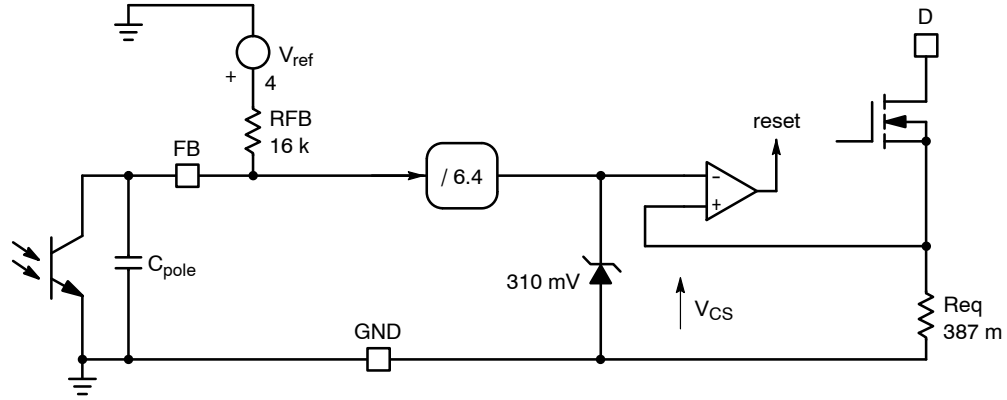

Figure 3. The NCP1027 Arrangement Follows That of the NCP101X Series. Here, a Simplified View

Small-Signal Modeling of the Switcher

The fact that all functions (sensing, switching etc.) are internally performed, does not change the small-signal transfer function of a converter implementing such a switcher. What is important are the values of some of the key elements inside the switcher. These are the pull-up resistor, the internal divider ratio and, finally, the equivalent sense resistor value. Once we have these values on hand, we can start looking at the small-signal response of the converter under study. The technical literature abounds with ready-to-use results of popular converter transfer functions. Ref. [2] details some of them on page 225. For a flyback converter, we need to identify the static gain G_0, the various frequency poles and zeros f_{p1}/f_{z1} plus a right-half-plane zero f_{z2} (RHPZ) if operated in CCM. First, we need to differentiate the operating mode, Discontinuous Conduction Mode (DCM) or Continuous Conduction Mode (CCM) which influences the static gain G_0 but also the position of the poles and zeros.

DCM

$$G_0 = \frac{1}{G_{FB}R_{sense}}\sqrt{\frac{L_pR_{load}F_{sw}}{2}} \quad \text{(eq. 4)}$$

$$f_{p1} = \frac{1}{\pi R_{load}C_{out}} \quad \text{(eq. 5)}$$

$$f_{z1} = \frac{1}{2\pi R_{ESR}C_{out}} \quad \text{(eq. 6)}$$

CCM

$$G_0 = \frac{R_{load}}{R_{sense}G_{FB}N}\frac{1}{\frac{(1-D)^2}{\tau_L} + 2M + 1} \quad \text{(eq. 7)}$$

$$f_{p1} = \frac{\frac{(1-D)^3}{\tau_L} + 1 + D}{2\pi R_{load}C_{out}} \quad \text{(eq. 8)}$$

$$f_{z1} = \frac{1}{2\pi R_{ESR}C_{out}} \quad \text{(eq. 9)}$$

$$f_{z2} = \frac{(1-D)^2\,R_{load}}{2\pi D L_pN^2} \quad \text{(eq. 10)}$$

Where:

L_p is the primary inductance of the flyback transformer

N is the flyback transformer turns ratio N_p:N_s

C_{out} is the output capacitor

G_{FB} represents the internal feedback to current sense divider

R_{ESR} is the output capacitor equivalent series resistor

D is the operating duty-cycle

R_{sense} is the internal sense resistor as described above

M is the conversion ratio

$$\tau_L = \frac{2L_pN^2}{R_{load}T_{sw}}$$

Please note that the CCM equations ignore the presence of ramp compensation and do not include the presence of the sub harmonic poles located at half the switching frequency. Regarding the DCM equations, we did not consider the presence of the high frequency pole and the RHPZ though they exist in discontinuous.

Compensating a CCM Converter

Let us assume we have a CCM flyback converter operating with the following component values:

$V_{in,min}$ = 120 V

V_{out} = 12 V

P_{out} = 10 W

R_{load} = 14.4 Ω

F_{sw} = 65 kHz

C_{out} = 3000 μF

R_{ESR} = 100 mΩ

L_p = 3 mH

N = 0.177

For various considerations, we have selected a NCP1027 to perform the switching task. From its data-sheet specifications and the above lines, we will extract the relevant information we need:

G_{FB} = 6.4

R_{sense} = 387 mΩ

R_{pullup} = 16 kΩ

We now have two choices: either we go through analytical calculations only and we draw our Bode plot by hand or, second option, we can use a dedicated SPICE model to avoid using equations. Let's try to combine both approaches, at least to confirm that our SPICE model delivers results we can trust for the analysis! From Equations 7 to 10, we have:

$$M = \frac{V_{out}}{NV_{in}} = \frac{12}{0.177 \times 120} = 0.564 \quad \text{(eq. 11)}$$

$$D = \frac{V_{out}}{V_{out} + NV_{in}} = \frac{12}{12 + 0.177 \times 120} = 0.361 \quad \text{(eq. 12)}$$

$$\tau_L = \frac{2\,L_pN^2}{R_{load}T_{sw}} = \frac{2 \times 3\,m \times 0.177^2}{14.4 \times 15.4\,\mu} = 0.848 \quad \text{(eq. 13)}$$

$$G_0 = \frac{R_{load}}{R_{sense}G_{FB}N}\frac{1}{\frac{(1-D)^2}{\tau_L} + 2M + 1} = \frac{14.4}{0.387 \times 6.4 \times 0.177} \times \frac{1}{\frac{(1-0.361)^2}{0.848} + 2 \times 0.564 + 1} = 12.58 \quad \text{(eq. 14)}$$

$$20\ \log_{10} G_0 = 22\ \text{dB} \quad \text{(eq. 15)}$$

$$f_{p1} = \frac{\frac{(1-D)^3}{\tau_L} + 1 + D}{2\pi R_{load}C_{out}} = \frac{\frac{(1-0.361)^3}{0.848} + 1 + 0.361}{6.28 \times 14.4 \times 3\ \text{m}} = 6.2\ \text{Hz} \quad \text{(eq. 16)}$$

$$f_{z1} = \frac{1}{2\pi R_{ESR}C_{out}} = \frac{1}{6.28 \times 100\ \text{m} \times 3\ \text{m}} = 530.5\ \text{Hz} \quad \text{(eq. 17)}$$

$$f_{z2} = \frac{(1-D)^2\ R_{load}}{2\pi D L_p N^2} = \frac{(1-0.361)^2 \times 14.4}{6.28 \times 0.361 \times 3\ \text{m} \times 0.177^2} = 27\ \text{kHz} \quad \text{(eq. 18)}$$

With these results on hand, we can now try to run a simulation using an auto-toggling average model as the one derived in Ref. [2]. Its open-loop configuration appears in Figure 4:

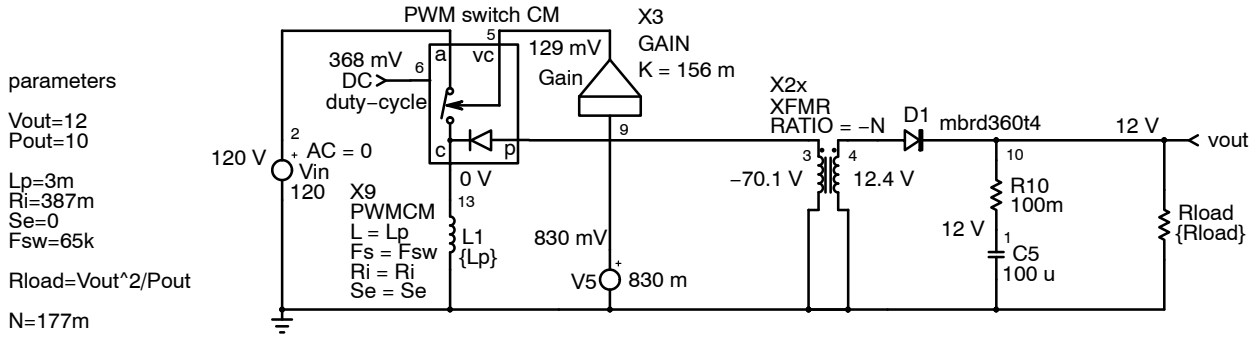

Figure 4. The Open-Loop Configuration of a Flyback Converter Using the NCP1027

You can note a slightly higher duty-cycle (36.8%) linked to the presence of the output diode whose forward drop affects the efficiency. Figure 5 displays the Bode plot obtained when using the above configuration.

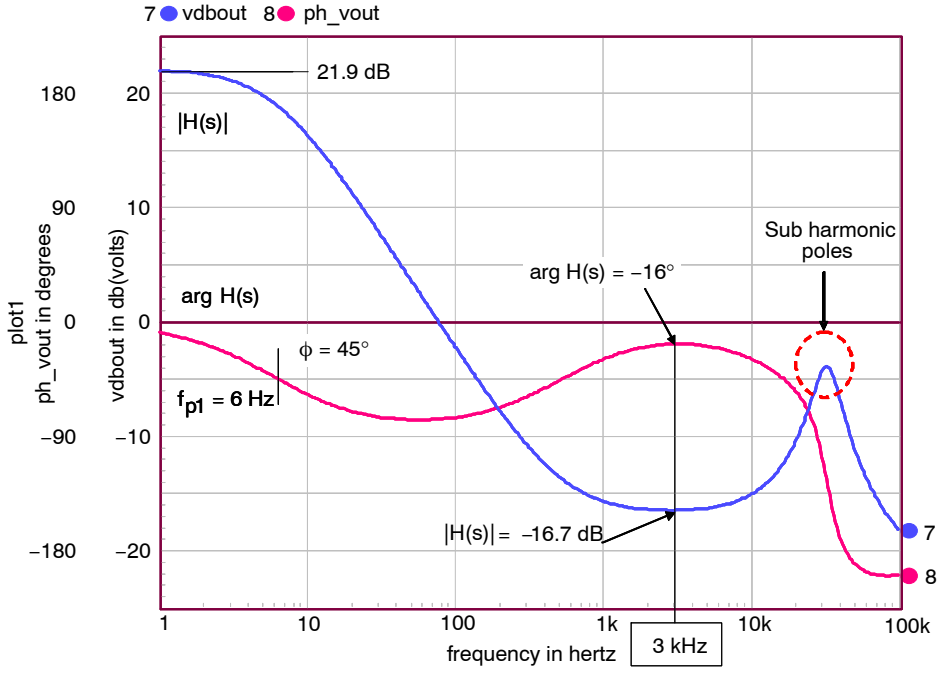

Figure 5. The Open-loop Bode Plot Obtained from Figure 4 Simulation which Confirms our Calculations

Please note the presence of sub harmonic pole properly predicted by the model despite a duty-cycle below 50%. However, no damping is necessary in our case thus ramp compensation is not needed.

The RHPZ expressed by Equation 18 limits the available bandwidth. Practically, in a CCM design, we recommend a cross over frequency which stays below 30% of the worse case RHPZ position. Beyond this value, the phase stress induced by the zero might become difficult to manage. In our example, 30% of the RHPZ implies a possible cross over frequency up to 8 kHz. For the sake of simplicity, we will limit our needs to a cross over value of 3 kHz where the power stage phase lag is minimum. The idea is now to extract the power stage insertion loss at 3 kHz and provide the necessary compensation gain to reach 0 dB at 3 kHz. From Figure 5, the gain loss is around –16.7 dB (0.146). Analytically, we could also derive it this way:

$$|H(s)| \approx \left| G_0 \frac{\left(1 - \frac{s}{s_{z2}}\right)\left(1 + \frac{s}{s_{z1}}\right)}{1 + \frac{s}{s_{p1}}} \right| = G_0 \frac{\sqrt{1 + \left(\frac{f_c}{f_{z2}}\right)^2}\sqrt{1 + \left(\frac{f_c}{f_{z1}}\right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_{p2}}\right)^2}} \quad \text{(eq. 19)}$$

$$|H(3\ \text{kHz})| = 12.6 \times \frac{\sqrt{1 + \left(\frac{3\ k}{27\ k}\right)^2}\sqrt{1 + \left(\frac{3\ k}{530}\right)^2}}{\sqrt{1 + \left(\frac{3\ k}{6.2}\right)^2}} = 0.149 \quad \text{(eq. 20)}$$

What is also important to know is the phase shift induced by the power stage at 3 kHz. From the Bode plot, we read –18°. We can also obtain it analytically keeping in mind that Equation 19 does not include the sub harmonic poles contribution:

$$\arg\ H(f_c) = \tan^{-1}\left(\frac{f_c}{f_{z1}}\right) + \tan^{-1}\left(-\frac{f_c}{f_{z2}}\right) - \tan^{-1}\left(\frac{f_c}{f_{p1}}\right) = -16° \quad \text{(eq. 21)}$$

Based on these above numbers, we will need to provide +16.7 dB of gain (≈7) at the selected 3 kHz frequency and almost no phase boost given the weak phase rotation brought by the power stage.

Compensating with the TL431

The TL431 lends itself very well for a type−2 compensation where we need a pole at the origin, a single pole and a single zero. The configuration of such system appears in Figure 6. As shown in Ref. [2], it is possible to show that the poles and zeros locations around Figure 6 configuration obey the following expressions:

$$G = \frac{R_{pullup}}{R_{LED}} CTR \quad \text{(eq. 22)}$$

$$f_{po} = \frac{1}{2\pi R_{upper} C_{zero}} \quad \text{(eq. 23)}$$

$$f_z = \frac{1}{2\pi R_{upper} C_{zero}} \quad \text{(eq. 24)}$$

$$f_p = \frac{1}{2\pi R_{pullup} C_{pole}} \quad \text{(eq. 25)}$$

Where R_{pullup} is the internal pull-up resistor and CTR is the optocoupler Current Transfer Ratio.

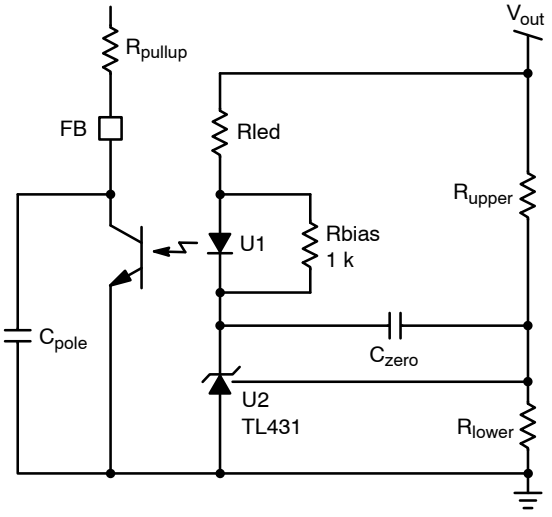

Figure 6. A TL431 is used to implement a type-2 compensator. For noise immunity reasons, make sure the C_{pole} capacitor is wired very close to the switcher FB and GND pins.

The first thing to fix is the divider ratio R_{upper} and R_{lower}. If we select a 250 μA bridge current (noise immunity is correct and input bias errors are minimized), the network values are easily found:

$$R_{lower} = \frac{2.5}{250\ \mu} = 10\ k\Omega \quad \text{(eq. 26)}$$

$$R_{upper} = \frac{12 - 2.5}{250\ \mu} = 38\ k\Omega \quad \text{(eq. 27)}$$

If we consider a CTR of 1 for our optocoupler, we can already calculate the LED resistor value:

$$R_{LED} = \frac{R_{pullup}}{G}CTR = \frac{16\ k}{7} \times 1 = 2.3\ k\Omega \quad \text{(eq. 28)}$$

R_{LED} not only fixes the loop gain but it also limits the current excursion in the optocoupler LED when the TL431 is fully biased (V_{out} above the target). In that case, as its cathode-anode voltage drops to 2.5 V, R_{LED} must be designed to offer enough current capability in the LED during these transient events. It thus becomes another design parameter. For 12 V output voltages, this is usually not a problem, but for 5 V designs, it can be a challenge especially for low CTR optocouplers. Please note the presence of R_{bias} which makes sure the TL431 receives, at least, a 1 mA bias current whatever the primary feedback current value is. This added bias current is important to make sure the TL431 operates in a favorable zone where its open-loop gain is the highest.

Finally, the optocoupler includes a pole whose position depends on the pull-up resistor and other factors. This pole lags the phase and can degrade the margin when it appears in the loop path. It is the designer duty to make sure the needed phase margin is not compromised once this optocoupler is installed.

To boost the phase at the crossover frequency, we have to install poles and zeros. The k-factor offers a possible method to automatically calculate the poles and zeros location based on a selected cross over frequency and a desired phase boost, right at this point. The method works fine for 1st order systems, such as DCM or CCM flyback converter operating in current mode. Even if the k-factor is not a panacea, it will at least help the inexperienced user find a stable point quickly. Once the component values are found, you will need to go in the laboratory and perform a bandwidth measurement anyway to make sure the assumptions we took during the calculations lead to the adequate phase/gain margins. Without entering into the details on how the method was obtained [2], we first compute the necessary phase boost:

$$Boost = PM - PS - 90 \quad \text{(eq. 29)}$$

Where PM is the phase margin we are looking for (70° in our example). PS represents the phase shift brought by the power stage at the cross over frequency (–16°) and –90 accounts for the origin pole phase rotation. Once the numbers are plugged in, we find a boost of:

$$Boost = 70 + 16 - 90 = -4° \quad \text{(eq. 30)}$$

A value below 0 in this particular example shows that no phase boost is actually needed since the power stage phase shift is low at the cross over point. As a matter of fact, a simple type 1 would do the compensation job here which corresponds to a k of 1. Let's proceed with the calculation of the k coefficient value:

$$k = \tan\left(\frac{boost}{2} + 45\right) \approx 1 \quad \text{(eq. 31)}$$

The k-factor now recommends to evenly spread the pole and the zero by choosing the cross over frequency as the geometric mean between them. As no phase boost is required and k is 1, the pole and zero will simply be coincident at 3 kHz:

$$f_p = kf_c = 1 \times 3\ k = 3\ kHz \quad \text{(eq. 32)}$$

$$f_z = \frac{f_c}{k} = \frac{3\ k}{1} = 3\ kHz \quad \text{(eq. 33)}$$

Applying Equations 23 – 25, we obtain the following values on the TL431:

$$C_{zero} = \frac{1}{2\pi R_{upper} f_z} = \frac{1}{6.28 \times 38\ k \times 3\ k} = 1.4\ nF \quad \text{(eq. 34)}$$

$$C_{pole} = \frac{1}{2\pi R_{pullup} f_p} = \frac{1}{6.28 \times 16\ k \times 3\ k} = 3.3\ nF \quad \text{(eq. 35)}$$

We can now take these values and capture a fully closed-loop circuitry as it appears in Figure 7:

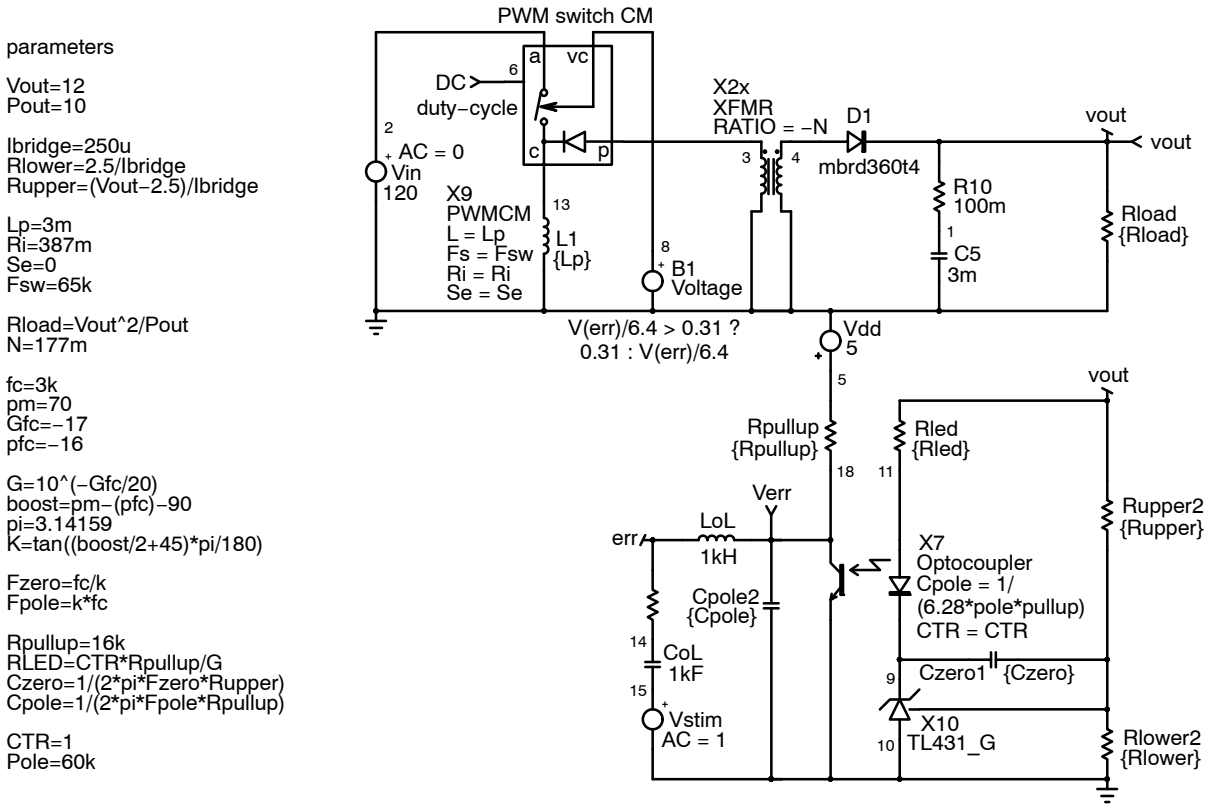

Figure 7. The Complete Converter Featuring the TL431 used to Control the Feedback Loop

In this sheet, all parameters calculations are automated on the left side. The optocoupler parameters are purposely disabled for the simplicity of the analysis. They should actually be characterized and the associated pole must take place in the loop study [2].

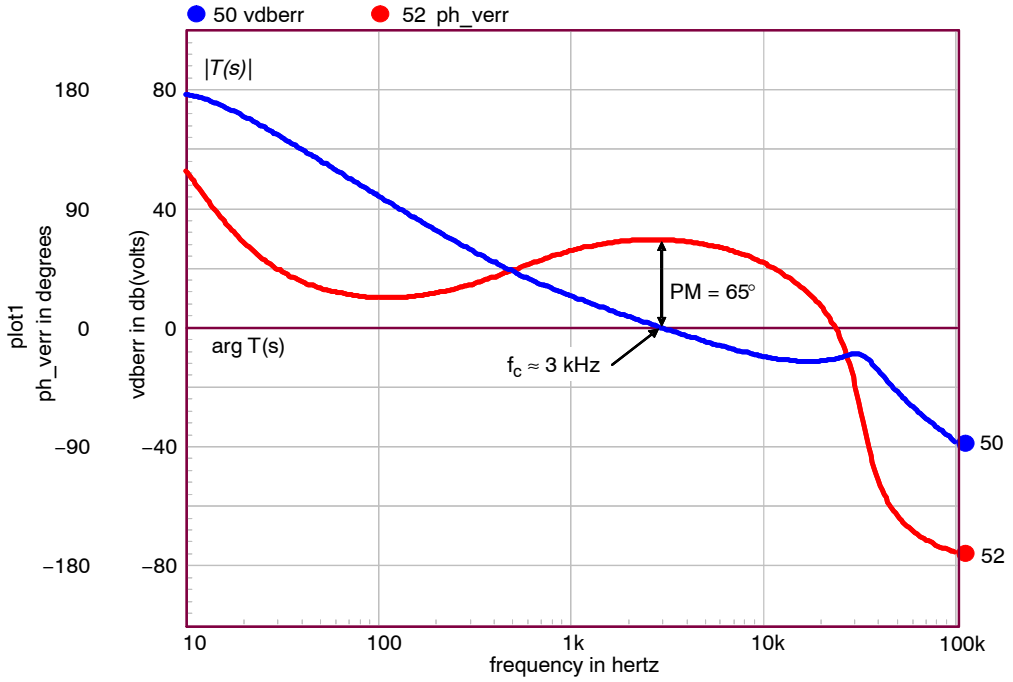

Figure 8. The Compensated Loop Gain T(s) once the Type-1 Circuit has been Implemented with the TL431

As Figure 8 testifies, the compensated loop gain looks stable with a phase margin of 65° at the crossover frequency.

"If I do not have the time to run simulations and analytical calculations?" Well, it is not advised to proceed this way but a simple quick and dirty compensation is to place a 100 nF capacitor for C_{zero}, put R_{LED} to 1 kΩ and C_{pole} to 10 nF. It won't be an optimally compensated design, but it should at least help you debug the board during the test experiments. Of course, you will still have to measure the loop and make sure enough phase margin is provided at the cross over point whatever input and output conditions.

Compensating with the TL431, DCM

In DCM, the converter remains a 1st order system and there are no sub harmonic poles. Let's assume we have the following converter design, actually similar to the previous one but where the primary inductor has been reduced. What inductor value shall we use to enter DCM? Let's calculate the critical value:

$$L_{p,crit} = \frac{R_{load}}{2F_{sw}N^2}\left(\frac{V_{in}}{V_{in} + \frac{V_{out}}{N}}\right)^2 = \frac{14.4}{2 \times 65\,k \times 0.177^2}\left(\frac{120}{120 + \frac{12}{0.177}}\right)^2 = 1.4\ mH \quad \text{(eq. 36)}$$

We can select a 1 mH inductor which will give us a static gain G_0 of 18.8 dB (D = 0.3 in DCM). Reconstructing the full Bode plot this time using Mathcad® (Figure 9) and involving the RHPZ with the second pole (Equations 4, 5 and 6), it gives us a gain loss at 3 kHz of –18 dB (0.126) with a phase deficit of –17°.

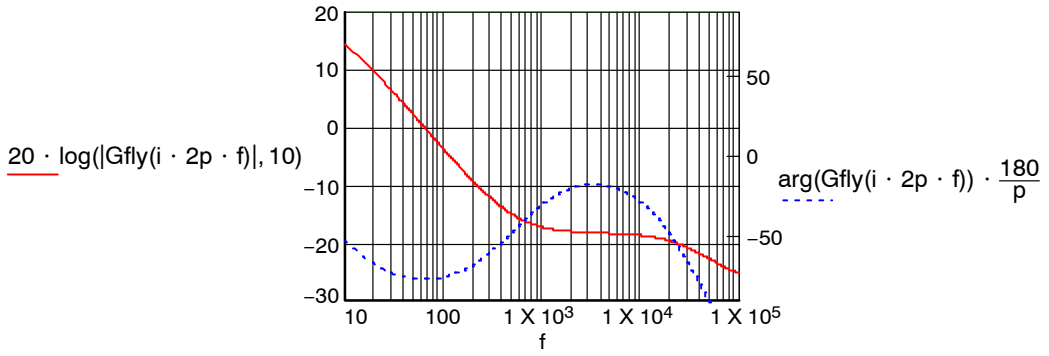

Figure 9. The Flyback Operated in DCM gives a First Order Response in the Low Frequency Portion

The method we disclosed in the previous lines still applies. We need to calculate the LED resistor to compensate the –18 dB loss which corresponds to a gain of +18 dB or a factor 8:

$$R_{LED} = \frac{R_{pullup}}{G}CTR = \frac{16\,k}{8} \times 1 = 2\,k\Omega \quad \text{(eq. 37)}$$

Given the low deficit of phase at the 3-kHz cross over frequency, we still use a type-1 compensator where both poles and zeros are coincident. Therefore, Equations 34 and 35 results are still valid for this DCM converter.

Primary Regulation with a Switcher

Primary regulation is often used in low-cost ac-dc or dc-dc applications. Despite the signal polarity on the feedback pin, a simple inversion can put it the right way. We have two options to generate an inverted signal. Figure 10 portrays an inversion made through a simple NPN transistor. Wired in a common-emitter configuration, the feedback pin is pulled down when the zener voltage is exceeded. The LED current and the collector current are now linked by the transistor beta which not only changes in temperature but also varies widely from lot to lot.

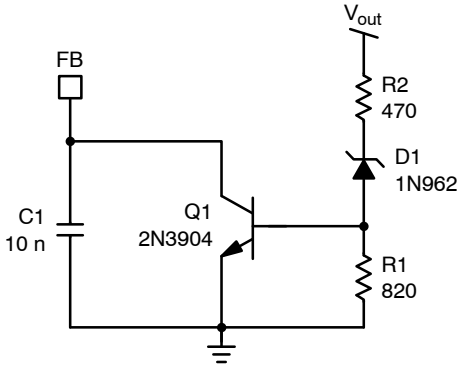

Figure 10. A Simple Transistor Can do the Feedback Job in a Non-isolated Converter configuration

The lower side resistor R_1 adjusts the bias current in the zener diode. It is recommended to check its data-sheet in order to select a current making it working far from its knee, e.g. with a bias current around the milliampere. R_2 sets the dc gain of the stage together with the pull-up resistor and the transistor beta. It also offsets the output voltage by the bias current:

$$V_{out} = V_{BE} + \frac{V_{BE}}{R_1}R_2 + V_Z \quad \text{(eq. 38)}$$

A possible alternative to improve the performance and the stability lies in using a current-mirror as described by Figure 11.

In this case, the zener current is simply conveyed on Q_1 collector without any gain if both transistors are properly paired. The best is to use a dual transistor device (e.g. a BC846BDW1T1G) where both transistors share a common die temperature and ensure the best performance for this kind of application. On the example, a 820 Ω resistor imposes a zener current of roughly 0.65/820 = 790 μA which can be further tweaked if necessary.

This configuration can also be applied to a buck converter such a the ones used in white goods applications where isolation is not necessary. Figure 12 details the approach:

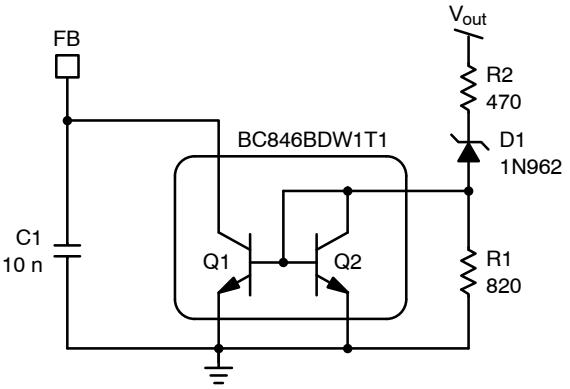

Figure 11. A Current Mirror Duplicates the LED Current as a Simple Optocoupler Device would Do

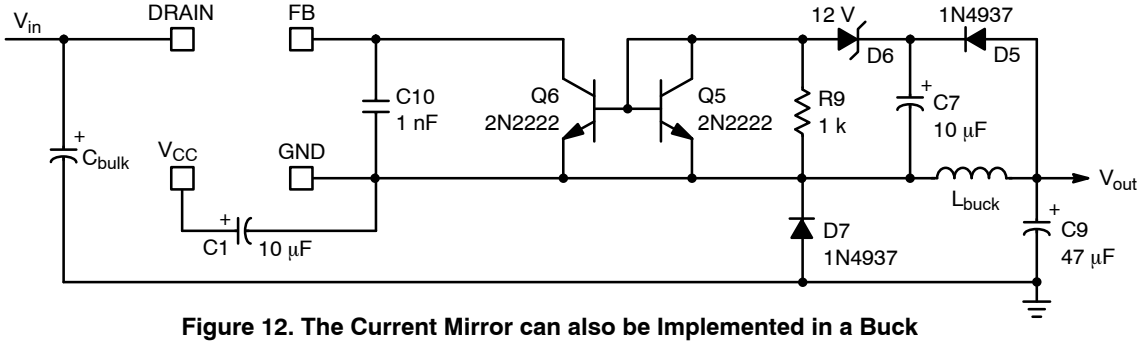

Figure 12. The Current Mirror can also be Implemented in a Buck Configuration, Here with a NCP101X Switcher

Conclusion

The stabilization of ON Semiconductor switcher series NCP101X or NCP1027 does not differ that much from other current-mode controllers as long as one understands the internal implementation. Once the designer knows the values of the current sense resistor and its associated feedback divider, the loop stability study can be quickly undertaken via classical analytical design techniques or by using a SPICE simulator and the available small-signal models.

References:

1. "Current Sensing Power MOSFETs", Application Note AND8093D, ON Semiconductor
2. C. Basso, "Switch Mode Power Supplies: SPICE Simulations and Practical Designs", McGraw-Hill 2008

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