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Designing Stable Control Loops for High Current Voltage Mode Synchronous Buck Converter with the NCP323X

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APPLICATION NOTE

Introduction

The NCP323X is a high current, high efficiency, voltage-mode synchronous buck converter which operates from 4.5 V to 21 V input and generates output voltages down to 0.6 V at up to 30 A. NCP323X utilizes voltage mode with voltage feed-forward control to respond instantly to V_{IN} changes and provide for easier compensation over the supply range of the converter. The typical application circuit is shown in Figure 1.

Despite the NCP323X's control loop is typical type III voltage feedback compensation, its design can't be overlooked, especially in telecom application. This article will show how to carry out the feedback compensation design.

To further ease the work of the design engineer, ON Semiconductor has developed a design tool CompCalc3 which is based on LabVIEW® Runtime Engine. The software plots the various ac responses based on the design component values.

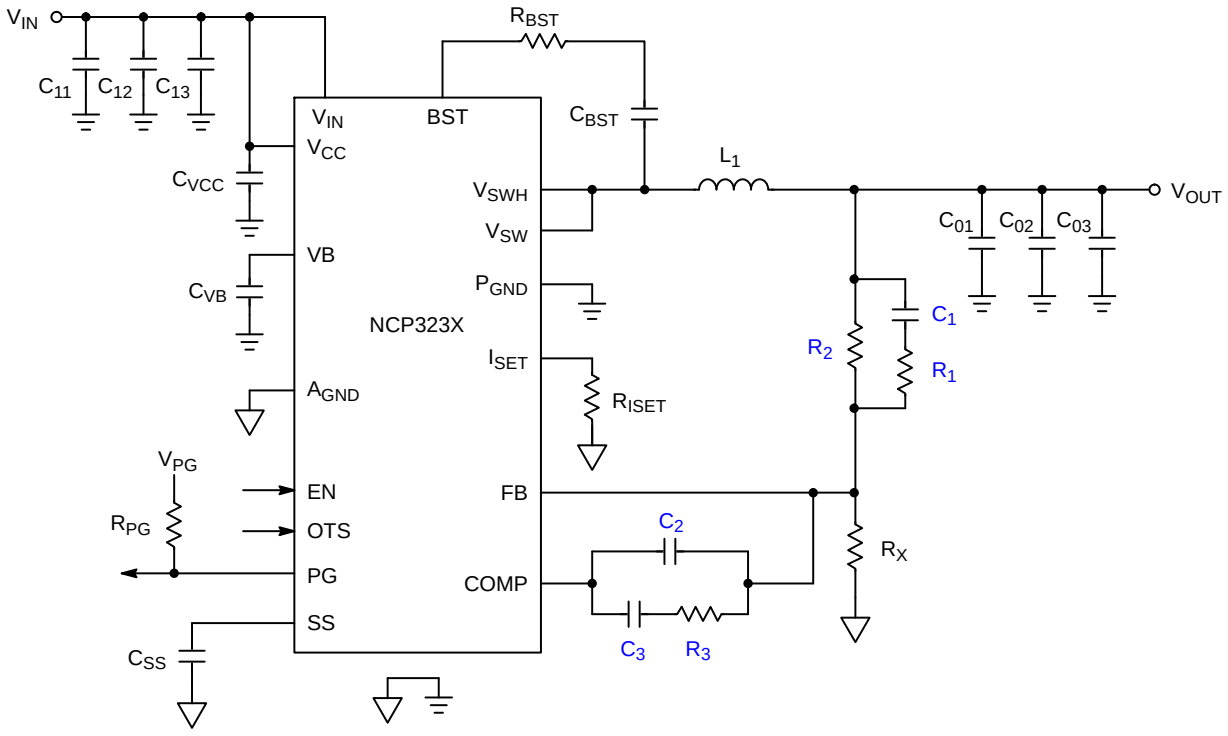

Figure 1. Typical Application Circuit with the NCP323X

Figure 2 presents a simplified diagram of a closed-loop controlled NCP323X. The converter is divided into three functional blocks for the convenience of modeling: the power stage, PWM block, and voltage feedback circuit.

Each functional block can be transformed into the respective small-signal model using various modeling techniques. The small-signal models of the three functional blocks are later merged to yield a complete small-signal model for the closed-loop controlled PWM converter.

The output voltage V_{out} is fed to a voltage feedback circuit, consisting of an op-amp, reference voltage V_{ref}, and two R−C impedance blocks. The output of the voltage feedback circuit is the control voltage, V_{ea}, which is used as the input signal for the PWM block. The voltage feedback circuit operates based on the principle of the negative feedback.

Table 1 list all products of NCP323X family and their feedback control loop design parameters.

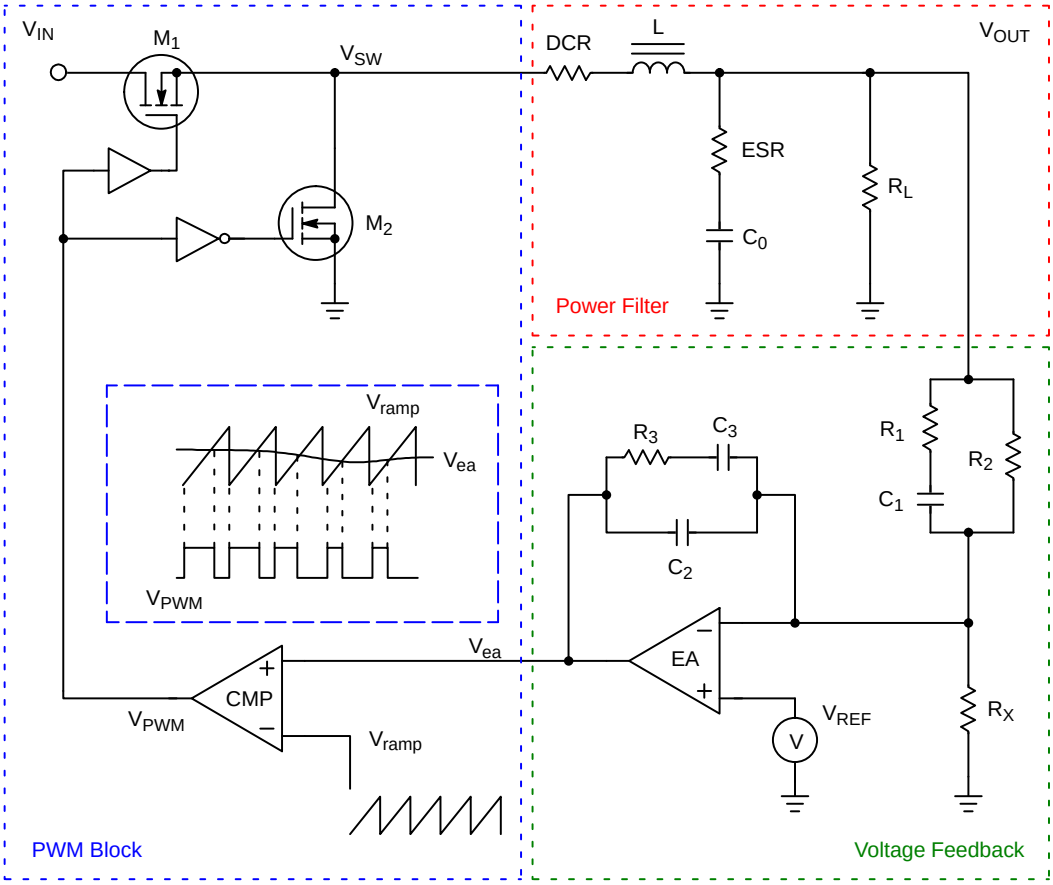

Figure 2. Three Function Blocks of NCP323X

Table 1. NCP323X FAMILY PARAMETERS RELATED TO FEEDBACK CONTROL LOOP DESIGN

Part Number	V_{ramp} Amplitude	EA Parameters	Operation Condition
NCP3231A	V_{IN}/6.6	Typ. GDB: 85 dB Min. GDB: 60 dB UGBW: 24 MHz	F_S = 500 kHz, 25 A
NCP3231	V_{IN}/6.6		F_S = 500 kHz, 25 A
NCP3232N	V_{IN}/6.6		F_S = 500 kHz, 15 A
NCP3230	V_{IN}/6.3		F_S = 500 kHz, 30 A
NCP3233	V_{IN}/5.4		V_{INX} = GND, F_S = 300/500 kHz/1 MHz, 20 A
	V_{IN}/1.4		V_{INX} = 3.3 V, F_S = 300/500 kHz/1 MHz, 20 A
NCP3235	V_{IN}/6.5		F_S = 550 kHz/1 MHz, 15 A

PWM Block

The PWM block in Figure 2 illustrates the operation of PWM control. The PWM block compares the control signal V_{ea} against the saw-tooth ramp signal, V_{ramp}, to generate the pulse-width modulated switch drive sign.

The constant small-signal gain of the PWM block is termed as the PWM gain or modulator gain F_m. The PWM gain is given by the inverse of the height of the ramp signal:

$$F_m = \frac{V_{SW}}{V_{ea}} = \frac{V_{IN}}{V_p} \quad \text{(eq. 1)}$$

Where V_p is the amplitude of V_{ramp}.

This simple result is the outcome of the fundamental assumption that the control voltage V_{ea} does not vary widely within one switching period and only changes slowly over several switching periods (the switch would produce the open-circuit, rail-to-rail square wave $V_{sw} = D \cdot V_{IN}$ with the duty cycle $D = V_{ea}/V_p$, or in total $V_{sw} = (V_{IN}/V_p) \cdot V_{ea}$).

NCP323X employs the input voltage feed-forward control method that makes the ramp signal amplitude is proportional to the input voltage, i.e. F_m is CONSTANT.

The input voltage feed-forward control method provides two main advantages: firstly the gain of the loop does not depend on the input voltage, the converter's behavior maintains the same for various input voltage; secondly higher ramp signal amplitude can mitigate the parasitic pulses due to the higher noise induced by higher input voltage switching.

Power Filter

The power filter is the well-known double pole single zero LC filter. Its transfer function is:

$$G_{LC\_Filter} = \frac{1 + \frac{s}{\omega_{esr}}}{1 + \frac{s}{Q\omega_0} + \frac{s^2}{\omega_0^2}} \quad \text{(eq. 2)}$$

Where,

$$\omega_{esr} = \frac{1}{C_0 \cdot ESR} \quad \text{(eq. 3)}$$

$$Q = R_L \cdot \sqrt{\frac{C_0}{L}} \quad \text{(eq. 4)}$$

$$\omega_0 = \frac{1}{\sqrt{L \cdot C_0}} \quad \text{(eq. 5)}$$

Open Loop Power Stage

The small-signal transfer function of open loop power stage which from the control input V_{ea} to the output V_{out} is:

$$G_{open\_loop} = F_m \cdot \frac{1 + \frac{s}{\omega_{esr}}}{1 + \frac{s}{Q\omega_0} + \frac{s^2}{\omega_0^2}} \quad \text{(eq. 6)}$$

Note that for $\omega << \omega_{esr}$, the LC structure exhibits the familiar second-order low-pass response LHP. However, at high frequencies, where C acts as a short circuit compared to its own ESR, the structure turns into a first-order LR circuit.

The borderline between the two cases is the frequency at which $|ZC(j\omega_{esr})| = DCR$. Aptly referred to as left-half-plane zero (LHPZ) frequency, ω_{esr} marks the point where slope changes from −40 dB/dec to −20 dB/dec, and phase is on its way to get boosted by +90°. Figure 3 shows the effect of the LHPZ on open loop power stage.

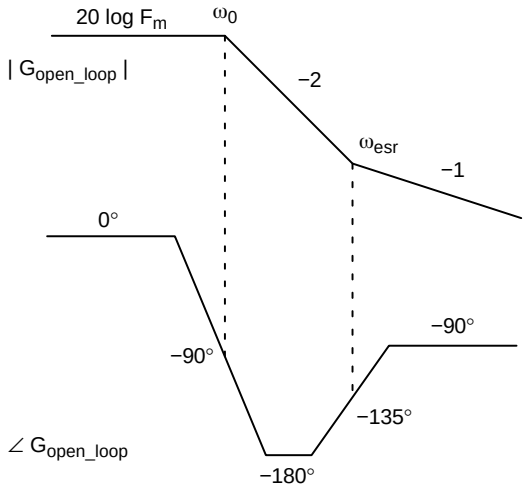

Figure 3. The Bode Plot of Open Loop Power Stage

Voltage Feedback

The negative feedback control is used through the feedback network, EA compensator network, and PWM to alleviate the variation caused by the disturbances.

A simple method that ensures the stable operation of the voltage-mode buck converter without modifying EA compensation is the use of an output capacitor with a high ESR value. Placing the ESR zero below the unit gain frequency can help improve the phase margin. If the ESR zero is placed at lower frequencies, a larger phase margin can be obtained to increase the stability. However, its low DC gain indicates poor load regulation and low output voltage accuracy, and the current flowing in or out of the capacitor induces a voltage drop across the ESR. A large voltage ripple and undershoot/overshoot voltage occur because of the IR drop voltage formed by the current variations across the ESR. Using the ESR zero can certainly simplify the compensation technique at the cost of regulation performance.

The voltage feedback network is composed of two feedback resistors R_2 and R_X. Using the feedback network, the output voltage information is fed back as error signal. The error signal between the feedback voltage and the reference voltage is amplified by the EA, which contains the compensation network.

In frequency compensation design, the crucial task is to design the compensated EA. Generally, achieving high DC gain at low frequencies, a 45° phase margin, and at least a 10 dB gain margin is demanded.

High DC gain and large bandwidth are need for regulation performance and fast transient response concurrently. To improve the regulation performance, an integrator can used to increase the DC gain. After using an integrator, the loop transfer function contains three poles (one pole at the origin is formed by the ideal integrator and two LHP poles, i.e. LC double poles). Then two additional LHP zeros are needed below the crossover frequency to increase the phase margin when a high DC gain is required at the same time. Type III compensation, which is commonly used in voltage-mode buck converters, is introduced to have two LHP zeros.

Type III Compensation

Type III compensation containing three LHP poles and two LHP zeros to obtain a high DC gain and a large bandwidth at the same time.

The small-signal transfer function of Type III compensation is:

$$G_{feed\_back} = \frac{K_c}{s} \cdot \frac{\left(1 + \frac{s}{\omega_{z1}}\right) \cdot \left(1 + \frac{s}{\omega_{z2}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right) \cdot \left(1 + \frac{s}{\omega_{p2}}\right)} \quad \text{(eq. 7)}$$

Where:

$$K_c = \frac{1}{R_2 \cdot (C_2 + C_3)} \quad \text{(eq. 8)}$$

$$\omega_{z1} = \frac{1}{R_3 \cdot C_3}, \quad \omega_{z2} = \frac{1}{(R_1 + R_2) \cdot C_1}$$
$$\omega_{p1} = \frac{1}{R_1 \cdot C_1}, \quad \omega_{p1} = \frac{1}{R_3 \cdot \frac{C_2 \cdot C_3}{C_2 + C_3}} \quad \text{(eq. 9)}$$

For the pole/zero pair, the phase boost is obtained from:

$$\text{boost} = \tan^{-1}\left(\frac{f}{f_{z1}}\right) + \tan^{-1}\left(\frac{f}{f_{z2}}\right) - \tan^{-1}\left(\frac{f}{f_{p1}}\right) - \tan^{-1}\left(\frac{f}{f_{p2}}\right) \quad \text{(eq. 10)}$$

The gain or attenuation G at crossover must have to compensate the close loop gain to 0-dB. Then the 0-dB crossover pole position is at

$$K_c = G \cdot \omega_{z1} \cdot \frac{\sqrt{1 + \left(\frac{f}{f_{p1}}\right)^2}\sqrt{1 + \left(\frac{f}{f_{p2}}\right)^2}}{\sqrt{1 + \left(\frac{f_{z1}}{f}\right)^2}\sqrt{1 + \left(\frac{f}{f_{z2}}\right)^2}} \quad \text{(eq. 11)}$$

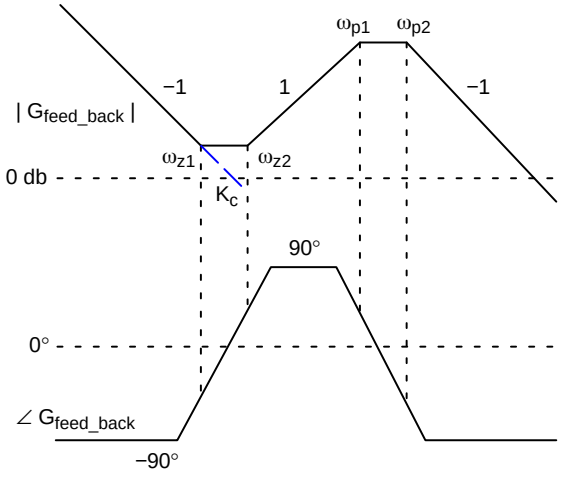

Figure 4. The Bode Plot of Type III Compensation

Figure 4 shows the asymptotic plot of the type III feedback compensation. The exact locations of the zeros and poles must be determined in consideration of their impacts on stability margins and closed-loop transfer functions.

With the type III compensation, the closed loop transfer function is expressed by

$$G_{system} = G_{open\_loop} \cdot G_{feed\_back} \quad \text{(eq. 12)}$$
$$= F_m \cdot \frac{K_c}{s} \cdot \frac{\left(1 + \frac{s}{\omega_{esr}}\right)\left(1 + \frac{s}{\omega_{z1}}\right)\left(1 + \frac{s}{\omega_{z2}}\right)}{\left(1 + \frac{s}{Q\omega_0} + \frac{s^2}{\omega_0^2}\right)\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)}$$

The typical type III compensation design guideline established as follows:

1. Select a crossover frequency f_c that is at least three to five times away from the resonating peak f_0 and at most one fifth away from the switching frequency f_s, i.e. 3~5 $f_{LC} \le f_c \le 0.2\ f_s$.

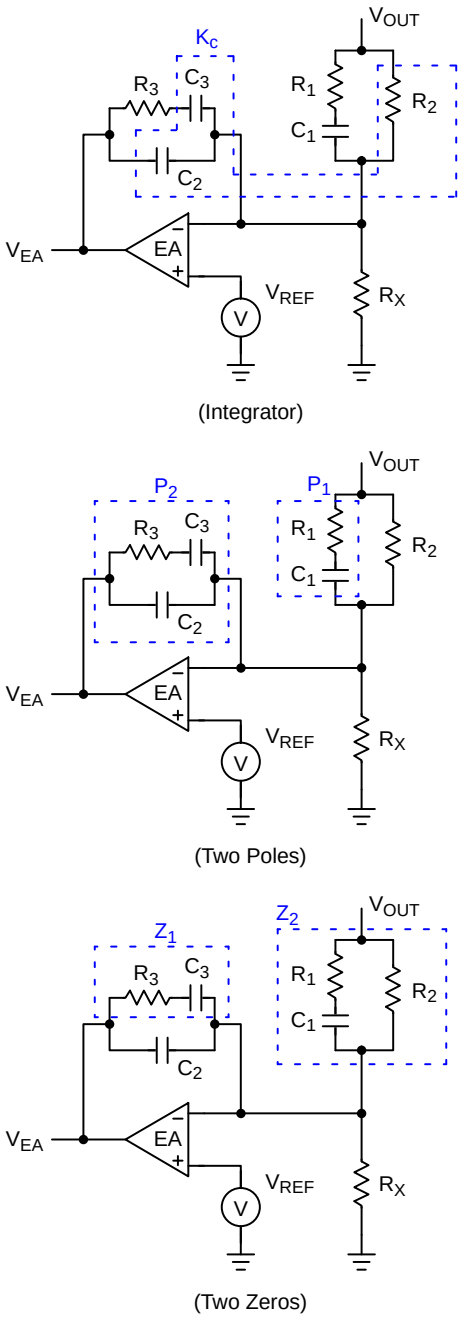

Figure 5. EA Design with Type III Compensation

2. Look the open loop transfer function G_{open_loop} and extract the gain deficiency G_{de} and phase PH at crossover frequency f_c. Then get compensator's amplification and phase boost with phase margin PM need provide: boost = PM − PH −90
3. Place the double zero pair near the LC network resonance frequency, usually between half of f_{LC} and f_{LC}, i.e. 0.5 $f_{LC} \le f_{z12} \le f_{LC}$.
4. If the ESR-linked zero appears before crossover, neutralize it by placing a pole right at its location. If the zero appears far away from the bandwidth, simply place the pole at half of the switching frequency. This first pole can then be moved to adjust the phase margin at the wanted value if necessary.
5. To force gain decrease at high frequency and ensure gain margin exists, place a second pole sufficiently high so that its presence does not hamper phase margin. It is usually placed at half of the switching frequency.
6. The 0-dB crossover pole K_c is computed in the integral term, which naturally depends on the wanted gain G at crossover.
7. Compute the compensation network (see Figure 5) components R_1, R_2, R_3, C_1, C_2, C_3.

$$R_3 = \frac{GR_2 f_{p2}}{f_{p2} - f_{z1}} \cdot \frac{\sqrt{1 + \left(\frac{f_c}{f_{p1}}\right)^2}\sqrt{1 + \left(\frac{f_c}{f_{p2}}\right)^2}}{\sqrt{1 + \left(\frac{f_{z1}}{f_c}\right)^2}\sqrt{1 + \left(\frac{f_c}{f_{z2}}\right)^2}} \quad \text{(eq. 13)}$$

8. Simulation and test the whole system bode plot with the compensation network components.

Design Example

This example describes the compensation design procedure for buck converter using NCP3231A. A design aid that allows users to determine component values quickly is available at www.onsemi.com.

DESIGN STEP 1:

Define Convertor Parameters

Input Voltage:	V_{IN}	12 V
Output Voltage:	V_{OUT}	0.8 V
Output Current:	I_{OUT}	20 A
Controller IC:	IC	NCP3231A
Osc. Voltage:	V_{ramp}	V_{IN}/6.6
Switching Frequency:	F_S	500 kHz
Total Out Capacitance:	C_O	470 μF
Total ESR:	ESR	0.5 mΩ
Output Inductance:	L	330 nH
Inductor DCR:	DCR	0.5 mΩ
Desired Phase Margin:	PM	60°

DESIGN STEP 2:

Select Crossover Frequency, f_c, at which the final closed loop crosses 0-dB. Identify the open loop gain deficiency, G_{de}, and the phase, PH, at f_c.

f_{LC} = 12.78 kHz
f_c = 60 kHz
G_{de} = −10.13 dB
PH = −166.16°

Compensator's amplification and phase boost at f_c need is

G = 10.13 dB
boost = 136.16°

DESIGN STEP 3:

Place zeros, f_{z1}, f_{z2}.

$f_{z1} = 0.5 \cdot f_{LC} = 6.39$ kHz
$f_{z2} = 1 \cdot f_{LC} = 12.78$ kHz
$f_{esr} = 677.26$ kHz

Due to $f_{esr} > f_s$, then place first pole at half of f_s.

$f_{p1} = 0.5 \cdot f_s = 250$ kHz

DESIGN STEP 4:

Compute the second pole, f_{p2}, by phase boost requirement.

$f_{p1} = 285.42$ kHz

The 0-dB crossover pole K_c is computed.

$K_c = 4.47$ kHz

DESIGN STEP 5:

Compute the compensation components (choose R2 as feedback component).

$R_2 = 20$ kΩ
$R_3 = 14.34$ kΩ
$C_3 = 1.74$ nF
$C_2 = 45.55$ pF
$R_1 = 937$ Ω
$C_1 = 594.8$ pF

Replace this calculated values with standard resisters and capacitors.

$R_2 = 20$ kΩ
$R_3 = 14.3$ kΩ
$C_3 = 1.8$ nF
$C_2 = 47$ pF
$R_1 = 931$ Ω
$C_1 = 560$ pF

The bode plot of type III system example is present in Figure 6 which includes open loop, feed-back, EA and close loop curves. The 60 kHz@60° requirement can be met.

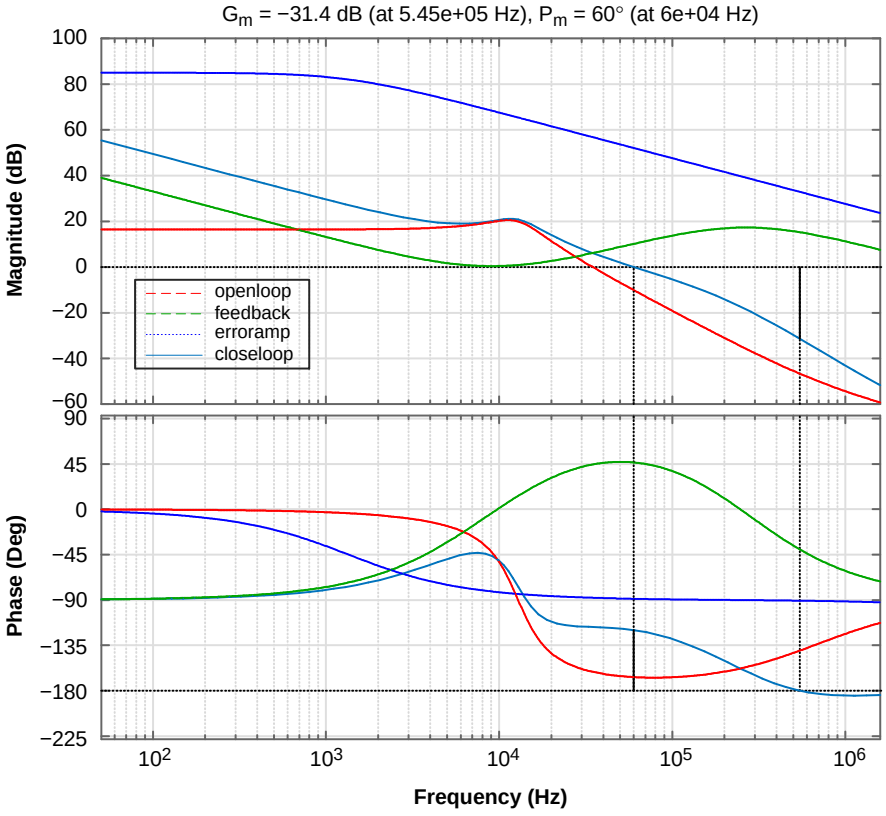

Figure 6. The Bode Plot of Type III System Example

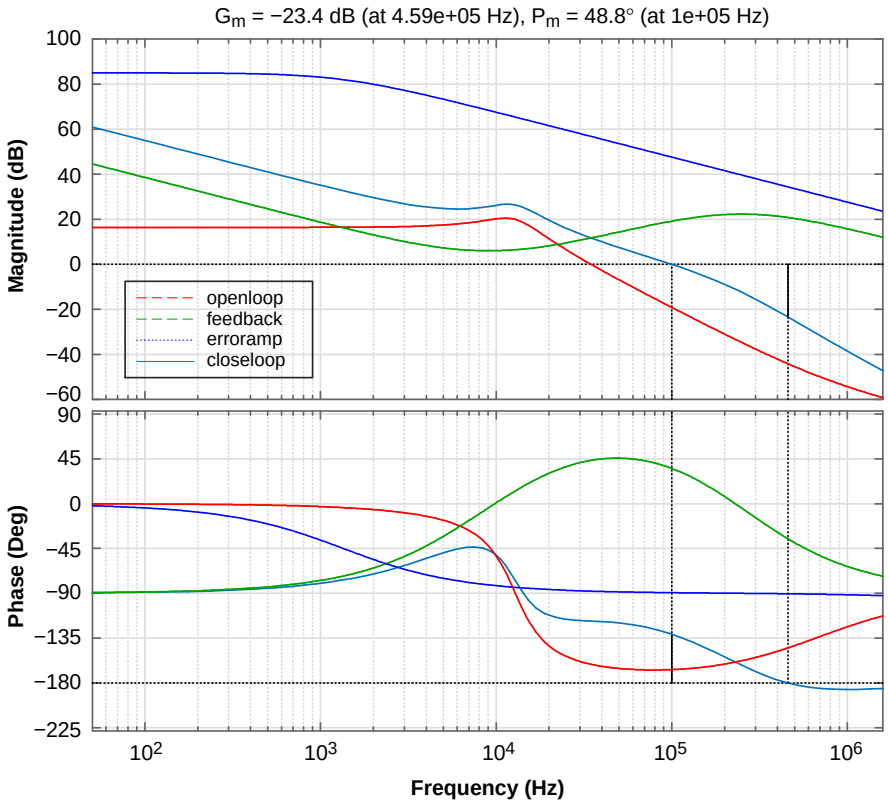

Figure 7. The Bode Plot of Type III System of 100 kHz Bandwidth

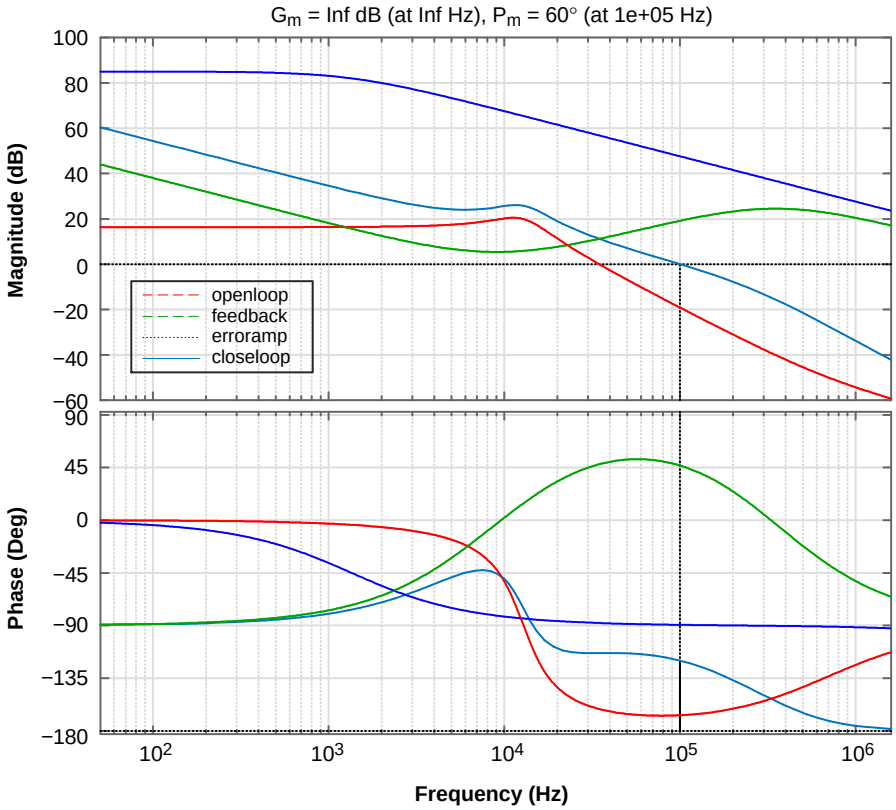

Figure 8. The Bode Plot of Revised Type III System of 100 kHz Bandwidth

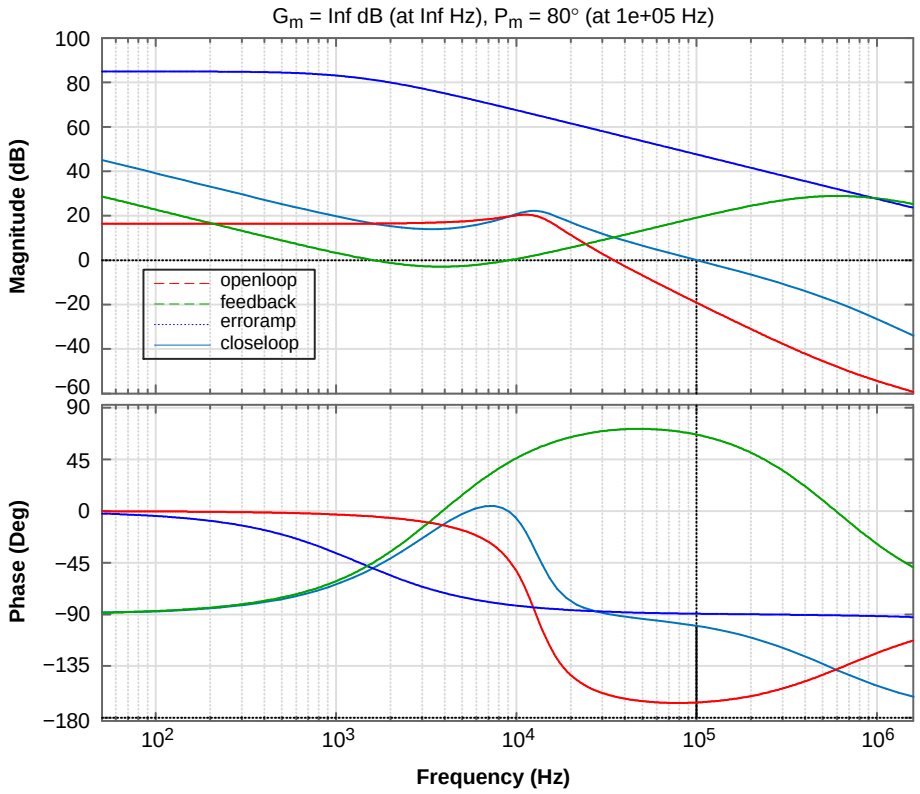

Figure 9. The Bode Plot of Type III System of 100 kHz Bandwidth and 80° Phase Margin

Discussion and Tips

Figure 7 present the bode plot with 100 kHz@60° requirement and the compensation components is

R_2 = 20 kΩ
R_3 = 27.4 kΩ
C_3 = 1 nF
C_2 = 24 pF
R_1 = 1.07 kΩ
C_1 = 560 pF

With zeros and poles

$f_{z1} = 0.5 \cdot f_{LC}$ = 6.39 kHz
$f_{z2} = 1 \cdot f_{LC}$ = 12.78 kHz
$f_{p1} = 0.5 \cdot f_s$ = 250 kHz
$f_{p2} = 0.5 \cdot f_s$ = 250 kHz

The result show that phase margin is 48.8° which can't meet 60° requirement. The improvement method is enlarging the separate distance of zeros and poles. One of the implement actions is setting the double poles to higher frequency positions and keep other parameters same, i.e.

f_{p1} = 288 kHz
f_{p2} = 425 kHz

The revised compensation components is

R_2 = 20 kΩ
R_3 = 25.5 kΩ
C_3 = 1 nF
C_2 = 15 pF
R_1 = 931 Ω
C_1 = 560 pF

Figure 8 present the revised bode plot which meet 100 kHz@60° requirement. Another implementation such as setting the double zeros to lower frequency positions also can get a similar PASS result which meet the requirement.

However, both of setting poles to higher frequency zone and frequency zeros to lower frequency zone have their drawbacks. Higher frequency poles degrade the noise immunity performance at high frequency zone; Lower frequency zeros make the loop gain smaller at low frequency zone which degrade the regulate accuracy and enlarge output voltage ripple.

Can this app-note's design method generate reasonable value for some people pursued so-called HIGHER PERFORMANCE requirement such as 100 kHz bandwidth and 80° phase margin? The answer is NOT SURE. We can have a try! Take implement action of both higher frequency poles and lower frequency zeros

$f_{z1} = 0.3 \cdot f_{LC}$ = 3.83 kHz
$f_{z2} = 0.3 \cdot f_{LC}$ = 3.83 kHz
$f_{p1} = 1.2 \cdot f_s$ = 600 kHz
$f_{p2} = 1.2 \cdot f_s$ = 600 kHz

The compensation components is

R_2 = 20 kΩ
R_3 = 7.15 kΩ
C_3 = 5.6 nF
C_2 = 36 pF
R_1 = 127 Ω
C_1 = 2.2 nF

Figure 9 present the theoretic bode plot with this setting. It seems meet the requirement. BUT, the green compensation gain curve encroach on the blue EA's open-loop gain curve (85 dB@24 MHz UGBW for NCP3231A) at the high frequency zone. This means the limit of the EA's gain has been reached and there is no more gain is available. The feedback function will roll off with one or more poles. The result will be that the desired loop compensation is not achieved, and the crossover and phase margin will be less than anticipated.

The compensation design is a tradeoff between bandwidth and phase margin which is related to the internal EA's performance. The poles and zeros placement for converter is also a tradeoff between speed and regulation performance. The beauty of loop compensation design is exactly this tradeoffs.

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