

NCP1093, NCP1094

Integrated IEEE 802.3at PoE-PD Interface Controller

Description

The NCP1093 and NCP1094 are members of ON Semiconductor's high power HIPO™ Power over Ethernet Powered Device (PoE-PD) product family and integrate an IEEE 802.3at PoE-PD interface controller.

Both variants incorporate the required functions such as detection, classification, under voltage lockout, inrush and operational current limit. A power good and NCLASS_AT signal have been added to guarantee proper enabling/disabling of the DC-DC controller for both type-I and type-II operation. In addition, the NCP1093 offers a programmable under-voltage while the NCP1094 provides an auxiliary pin for applications supporting auxiliary supplies.

The NCP1093 and NCP1094 are fabricated in a robust high voltage process and integrate a rugged vertical N-channel DMOS suitable for the most demanding environments and capable of withstanding harsh environments such as hot swap and cable ESD events.

The NCP1093 and NCP1094 complement ON Semiconductor's ASSP portfolio in industrial devices and can be combined with stepper motor drivers, CAN bus drivers and other high-voltage interfacing devices to offer complete solutions to the industrial and security market.

Features

- Fully Supports IEEE 802.3af/at Specifications
- Programmable Classification Current
- Support Two Event Classification-Signature
- Adjustable Under Voltage Lock Out (NCP1093 Only)
- Open-Drain Power Good Indicator
- 120 mA Typical Inrush Current Limit
- 680 mA Typical Operational Current Limit
- Pass Switch Disabling Input for Rear Auxiliary Supply Operation (NCP1094 Only)
- Over-temperature Protection
- Industrial Temperature Range -40°C to 85°C with Full Operation up to 125°C Junction Temperature
- 0.6 Ω Hot-swap Pass-switch
- Vertical N-channel DMOS Pass-switch Offers the Robustness of Discrete MOSFETs
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



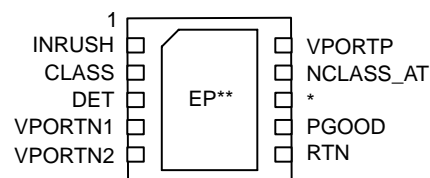
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DFN10
MN SUFFIX
CASE 485C

PIN CONFIGURATION



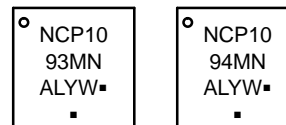
(Top View)

*NCP1093 = UVLO

NCP1094 = AUX

** Exposed pad should be connected to VPORTN

MARKING DIAGRAMS



NCP109xMN = Specific Device Code

A = Assembly Location

L = Wafer Lot

Y = Year

W = Work Week

▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

| Device | Package | Shipping† |
|-------------|--------------------|--------------------|
| NCP1093MNG | DFN10 (Pb-Free) | 120 Units / Tube |
| NCP1093MNRG | DFN10 (Pb-Free) | 3000 / Tape & Reel |
| NCP1094MNG | DFN10 (Pb-Free) | 120 Units / Tube |
| NCP1094MNRG | DFN10 (Pb-Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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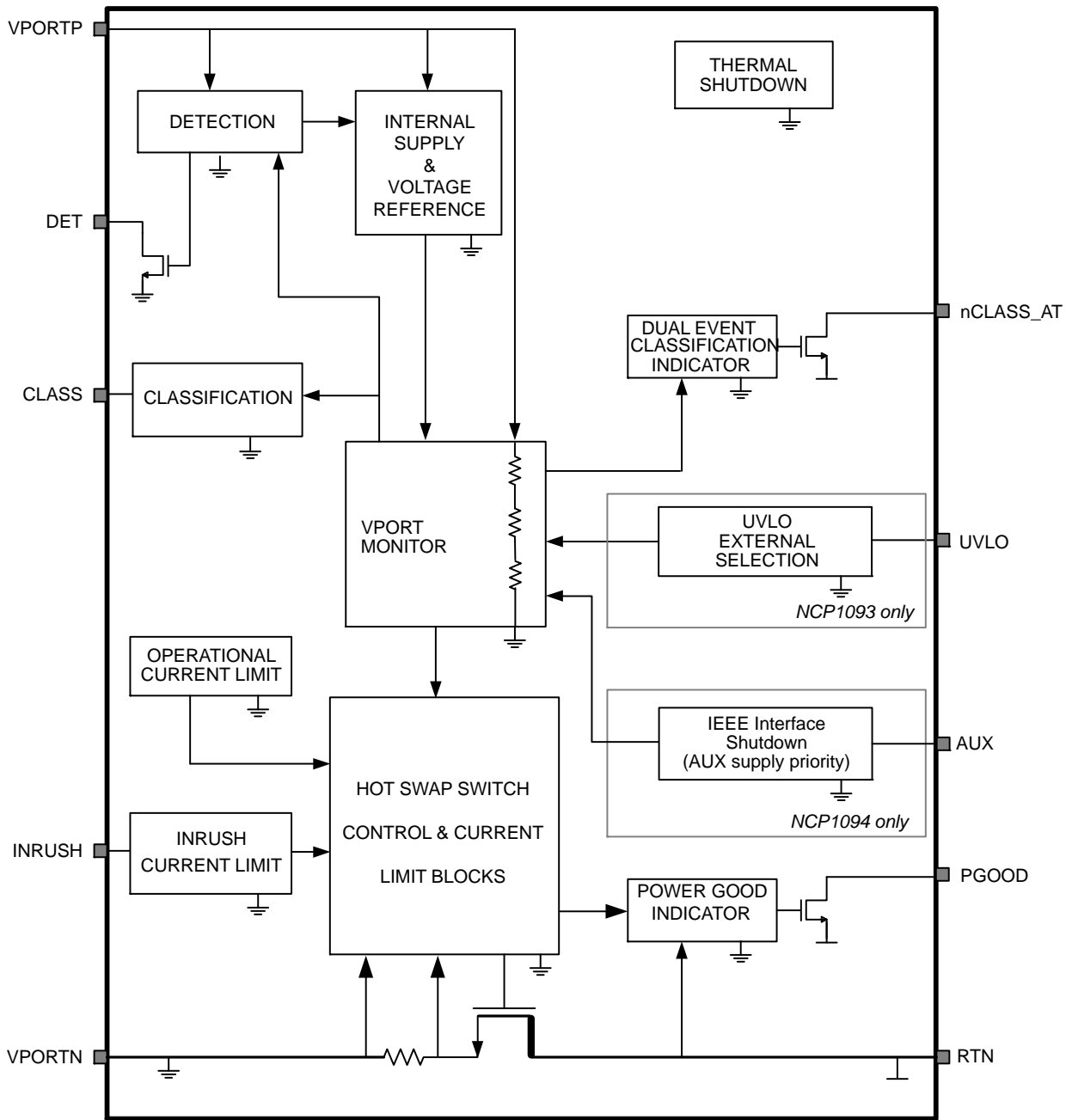


Figure 1. NCP1093/94 Functional Block Diagram

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Simplified Application Diagrams

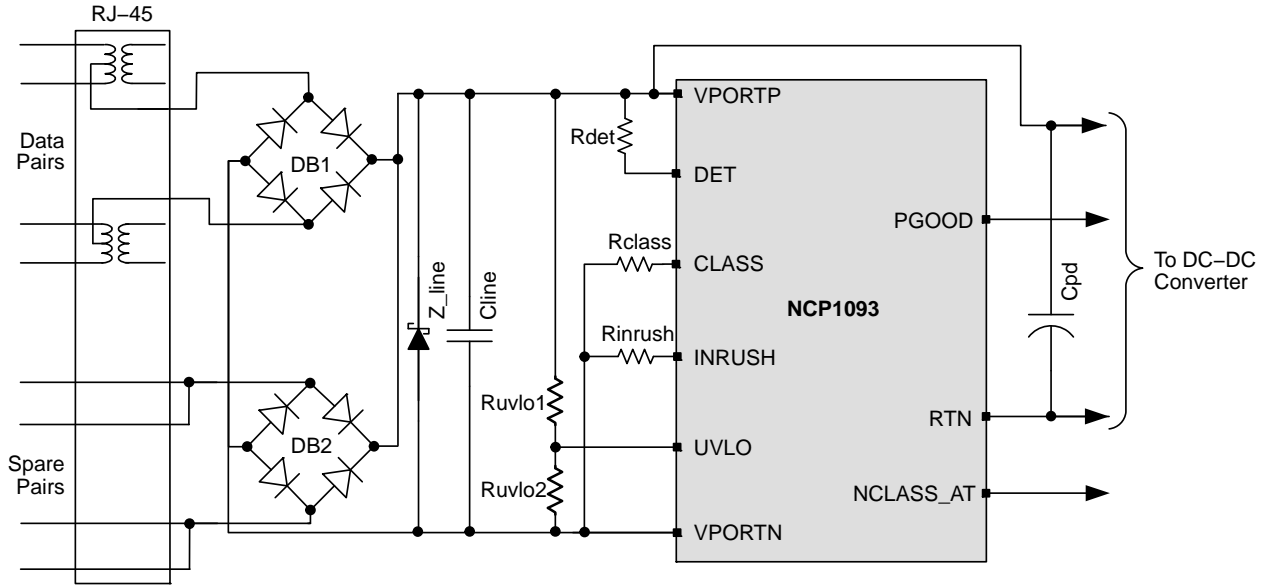


Figure 2. Typical Application Circuit using the NCP1093 with External UVLO Setting

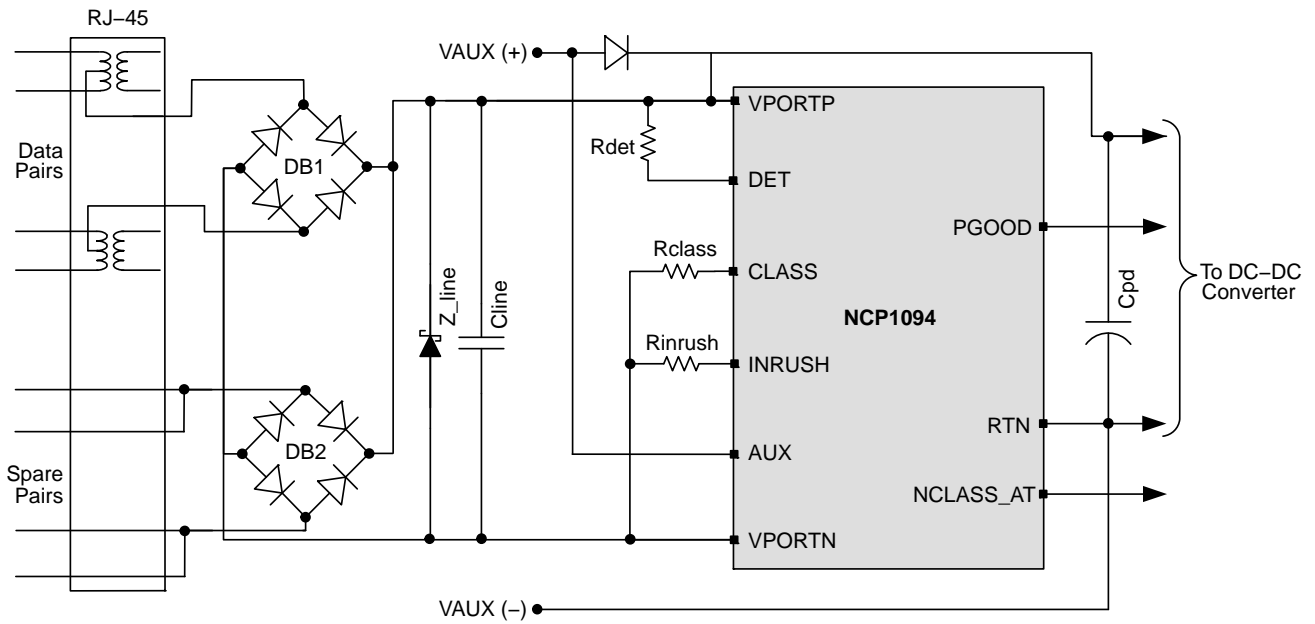


Figure 3. Typical Application Circuit using the NCP1094

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Table 1. PIN DESCRIPTION

| Name | Pin No. | | Type | Description |
|-------------|---------|---------|--------------------|---|
| | NCP1093 | NCP1094 | | |
| INRUSH | 1 | 1 | Output | Current limit programming pin. Connect a resistor between INRUSH and VPORTN. |
| CLASS | 2 | 2 | Output | Classification current programming pin. Connect a resistor between CLASS and VPORTN. |
| DET | 3 | 3 | Output, Open Drain | Detection pin. Connect a 24.9 kΩ resistor between DET and VPORTP for a valid PD detection signature. |
| VPORTN1 | 4 | 4 | Ground | Negative input power. Connected to the source of the internal pass-switch |
| VPORTN2 | 5 | 5 | Ground | Negative input power. Connected to the source of the internal pass-switch |
| RTN | 6 | 6 | Ground | DC-DC controller power return. Connected to the drain of the internal pass-switch |
| PGOOD | 7 | 7 | Output, Open Drain | Open Drain Power Good Indicator. Pin is in HZ mode when the power good signal is active. |
| UVLO | 8 | - | Input | Undervoltage lockout input. Voltage with respect to VPORTN. Connect a resistor-divider from VPORTP to UVLO to VPORTNx to set an external UVLO threshold. |
| AUX | - | 8 | Input | Auxiliary Pin. When this pin is pulled up, the Pass Switch is disabled and allows a supply transition from PSE to the rear auxiliary supply connected between VPORTP and RTN. |
| NCLASS_AT | 9 | 9 | Output | Active low enable signal used to verify high power operation |
| VPORTP | 10 | 10 | Input | Positive input power. Voltage with respect to VPORTN. |
| Exposed Pad | EP | EP | Ground | Exposed pad should be connected to VPORTN. |

Table 2. ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Min | Max | Units | Conditions |
|----------------------------------|--|------|-----|-------|---|
| VPORTP | Input power supply | -0.3 | 72 | V | Voltage with respect to VPORTN |
| RTN | Analog ground supply 2 | -0.3 | 72 | V | Pass-switch in off-state (voltage with respect to VPORTN) |
| CLASS | Analog output | -0.3 | 72 | V | Voltage with respect to VPORTN |
| INRUSH | Analog output | -0.3 | 3.6 | V | Voltage with respect to VPORTN |
| AUX | Analog input | -0.3 | 72 | V | Voltage with respect to VPORTN |
| UVLO | Analog input | -0.3 | 3.6 | V | Voltage with respect to VPORTN |
| PGOOD | Analog output | -0.3 | 72 | V | Voltage with respect to RTN |
| T _A | Ambient temperature | -40 | 85 | °C | |
| T _J | Junction temperature | - | 125 | °C | |
| T _J , T _{SD} | Junction temperature (Note 1) | - | 175 | °C | Thermal shutdown condition |
| T _{STG} | Storage Temperature | -55 | 150 | °C | |
| T _{θJA} | Thermal Resistance, Junction to Air (Note 2) | 50 | | °C/W | DFN-10 |
| ESD-HBM | Human Body Model | 2 | | kV | per EIA-JESD22-A114 standard |
| ESD-CDM | Charged Device Model | 500 | | V | per ESD-STM5.3.1 standard |
| ESD-MM | Machine Model | 200 | | V | per EIA-JESD22-A115-A standard |
| LU | Latch-up | ±100 | | mA | per JEDEC Standard JESD78 |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. T_J-T_{SD} allowed during error conditions only. It is assumed that this maximum temperature condition does not occur more than 1 hour cumulative during the useful life for reliability reasons.
2. Low θ_{JA} is obtained with 2S2P test board (2 signal – 2 plane). High θ_{JA} is obtained with double sideboard with minimum pad area and natural convection. Refer to Jedec JESD51 for details. The exposed pad must be connected to the VPORTN ground pin.

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Recommended Operating Conditions

Operating conditions define the limits for functional operation and parametric characteristics of the device. Note that the functionality of the device outside the operating conditions described in this section is not warranted. Operating outside the recommended operating conditions for extended periods of time may affect device reliability.

Table 3. OPERATING CONDITIONS (All values are with respect to VPORTN unless otherwise noted.)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|--------|-----------|-----|-----|-----|-------|------------|
|--------|-----------|-----|-----|-----|-------|------------|

INPUT SUPPLY

| | | | | | | |
|-------|----------------------|---|---|----|---|-------------------------|
| VPORT | Input supply voltage | 0 | – | 57 | V | VPORT = VPORTP – VPORTN |
|-------|----------------------|---|---|----|---|-------------------------|

SIGNATURE DETECTION

| | | | | | | |
|-------------|--|-----|-----|-----|---------------|--|
| Offset_det1 | $I_{(VPORTP)} + I_{(RTN)}$ | – | 2 | 5 | μA | VPORTP = RTN = 1.9 V Rdet = 24.9 K Ω |
| Sleep_det1 | $I_{(VPORTP)} + I_{(RTN)}$ | – | 15 | 21 | μA | VPORTP = RTN = 9.8 V Rdet = 24.9 K Ω |
| Offset_det2 | $I_{(VPORTP)} + I_{(RTN)} + I_{(DET)}$ | 73 | 77 | 81 | μA | VPORTP = RTN = 1.9 V Rdet = 24.9 K Ω |
| Sleep_det2 | $I_{(VPORTP)} + I_{(RTN)} + I_{(DET)}$ | 390 | 400 | 412 | μA | VPORTP = RTN = 9.8 V Rdet = 24.9 K Ω |

CLASSIFICATION

| | | | | | | |
|------------|--|-----|------|-----|---------------|---|
| Vcl_on | Classification current turn-on lower threshold | 9.8 | 11.3 | 13 | V | VPORTP rising |
| Vcl_off | Classification current turn-off upper threshold | 21 | – | 24 | V | VPORTP rising |
| Vclass_reg | Classification buffer output voltage | – | 9.8 | – | V | 13 V < VPORTP < 21 V |
| Icl_bias | $I_{(vportp)}$ quiescent current during classification | – | 600 | – | μA | I(class) excluded 13 V < VPORTP < 21 V |
| Iclass0 | Class 0: Rclass 4420 Ω (Note 3) | 0 | – | 4 | mA | 13 V < VPORTP < 21 V |
| Iclass1 | Class 1: Rclass 953 Ω (Note 3) | 9 | – | 12 | mA | 13 V < VPORTP < 21 V |
| Iclass2 | Class 2: Rclass 549 Ω (Note 3) | 17 | – | 20 | mA | 13 V < VPORTP < 21 V |
| Iclass3 | Class 3: Rclass 357 Ω (Note 3) | 26 | – | 30 | mA | 13 V < VPORTP < 21 V |
| Iclass4 | Class 4: Rclass 255 Ω (Note 3) | 36 | – | 44 | mA | 13 V < VPORTP < 21 V |
| V_mark | Mark event voltage range | 5.4 | – | 9.7 | V | VPORTP falling |
| I_mark | $I_{(VPORTP)} + I_{(Rdet)}$ during mark event range | 0.5 | – | 2 | mA | 5.4 V \leq VPORTP \leq 9.7 V |
| dR_mark | Input signature during mark event (Note 4) | – | – | 12 | k Ω | |
| Vreset | Classification Reset range | 4.3 | 4.9 | 5.4 | V | VPORTP falling |

NCLASS_AT 2 EVENT CLASSIFICATION INDICATOR

| | | | | | | |
|------------|------------------------------------|---|-----|-----|----|-----------------------------------|
| Inclass | $I_{(NCLASS_AT)}$ sinking current | – | – | 5 | mA | |
| Nclass_low | NCLASS_AT voltage output low | – | 0.2 | 0.5 | V | $I_{(NCLASS_AT)} = 2 \text{ mA}$ |

UVLO – INTERNAL SETTING – NCP1093/94

| | | | | | | |
|-------------|---------------------------|------|-----|----|---------------|----------------------|
| Vuvlo_on | Default turn on voltage | – | 37 | 40 | V | VPORTP rising |
| Vuvlo_off | Default turn off voltage | 29.6 | 31 | – | V | VPORTP falling |
| Vhyst_int | UVLO internal hysteresis | – | 6 | – | V | |
| Uvlo_filter | UVLO On / Off filter time | – | 100 | – | μs | For information only |

3. A tolerance of 1% on the Rclass resistor is included in the min/max values.

4. Measured with the 2 Point Measurement defined in the IEEE 802.3af standard with 5.4 V and 9.7 V the extreme values for V2 & V1.

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Table 3. OPERATING CONDITIONS (All values are with respect to VPORTN unless otherwise noted.)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|--|---|------|-----|------|-------|--|
| UVLO – EXTERNAL SETTING – NCP1093 ONLY | | | | | | |
| Vuvlo_pr | UVLO external programming range | 25 | – | 50 | V | VPORTP rising |
| Vuvlo_on2 | External UVLO turn on voltage | 1.14 | 1.2 | 1.26 | V | |
| Vhyst_off2 | External UVLO turn off voltage | 0.95 | 1 | 1.05 | V | |
| Uvlo_ipd | UVLO internal pull down current | – | 2.5 | – | μA | |
| AUXILIARY SUPPLY SETTING – NCP1094 ONLY | | | | | | |
| Aux_h | AUX input high level voltage | 3.1 | – | | V | |
| Aux_l | AUX input low level voltage | – | – | 0.6 | V | |
| Aux_pd | AUX internal pull down resistor | 100 | – | – | kΩ | For information only |
| PASS-SWITCH AND CURRENT LIMITING | | | | | | |
| Ron | Pass-switch Rds-on | – | 0.6 | 1 | Ω | Measured with I(RTN) = 200 mA |
| I_inrush | Inrush current with Rinrush = 169 kΩ | 75 | 120 | 170 | mA | Measured at RTN–VPORTN = 3 V |
| I_ilim | Operating current limit with Rinrush = 169 kΩ | 610 | 680 | 800 | mA | Current limit threshold |
| POWER GOOD INDICATOR | | | | | | |
| Vds_pgood_on | RTN–VPORTN threshold voltage required for power good status | 0.8 | 1 | 1.2 | V | RTN–VPORTN falling |
| Vds_pgood_off | RTN–VPORTN latching threshold voltage | 9 | 10 | 11 | V | RTN–VPORTN rising |
| Pgood_filter | PGOOD filter time | | 100 | | μs | Rising and falling / for information only |
| Ipgood | I(PGOOD) sinking current | – | – | 5 | mA | |
| Vpgood_low | PGOOD voltage output low | – | 0.2 | 0.5 | V | I(PGOOD) = 2 mA Voltage with respect to RTN |
| CURRENT CONSUMPTION | | | | | | |
| IvportP | I(VPORTP) internal current consumption | – | 600 | 900 | μA | VPORTP = 48 V |
| THERMAL SHUTDOWN | | | | | | |
| TSD | Thermal shutdown threshold | 150 | – | – | °C Tj | Tj = junction temperature |
| Thyst | Thermal hysteresis | – | 15 | – | °C Tj | Tj = junction temperature |
| THERMAL RATINGS | | | | | | |
| Ta | Ambient temperature | –40 | – | 85 | °C | |
| Tj | Junction temperature | – | – | 125 | °C | |

3. A tolerance of 1% on the Rclass resistor is included in the min/max values.

4. Measured with the 2 Point Measurement defined in the IEEE 802.3af standard with 5.4 V and 9.7 V the extreme values for V2 & V1.

Description of Operation

Powered Device Interface

The integrated PD interface supports the IEEE 802.3af defined operating modes: detection signature, current source classification, undervoltage lockout, inrush and operating current limits. The following sections give an overview of these previous processes.

Detection

During the detection phase, the incremental equivalent resistance seen by the PSE through the cable must be in the IEEE 802.3af standard specification range (23.70 kΩ to 26.30 kΩ) for a PSE voltage from 2.7 V to 10.1 V. In order to compensate for the non-linear effect of the diode bridge and satisfy the specification at low PSE voltage, the NCP1093/94 present a suitable impedance in parallel with the 24.9 kΩ Rdet external resistor. For some types of diodes (especially Schottky diodes), it may be necessary to adjust this external resistor.

The Rdet resistor has to be inserted between VPORTP and DET pins. During the detection phase, the DET pin is pulled to ground and goes in high impedance mode (open-drain) once the device exit this mode, reducing thus the current consumption on the cable.

Classification

Once the PSE device has detected the PD device, the classification process begins. In classification, the PD regulates a constant current source that is set by the external resistor RCLASS value on the CLASS pin. Figure 4 shows the schematic overview of the classification block. The current source is defined as:

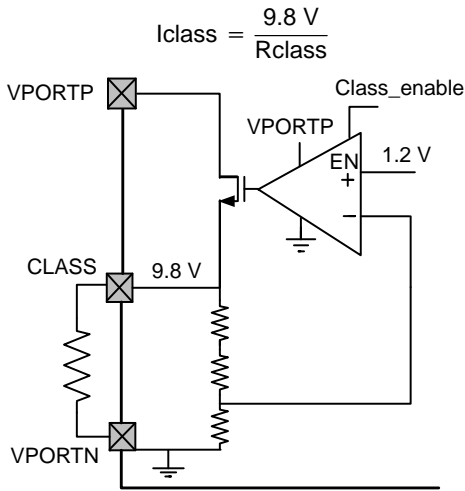


Figure 4. Classification Block Diagram

The NCP1093/94 is able to detect a dual event classification generated by a type 2 PSE, and flag it using its nCLASS_AT open drain indicator.

Power Mode

When the classification hand-shake is completed, the PSE and PD devices move into the operating mode.

Under Voltage Lock Out (UVLO)

The NCP1093/94 incorporate a fixed under voltage lock out (UVLO) circuit which monitors the input voltage and determines when to turn on the pass switch and charge the dc-dc converter input capacitor before the power up of the application.

The NCP1093 offers a fixed or adjustable Vuvlo_on threshold depending if the UVLO pin is used or not. In Figure 5, the UVLO pin is strapped to ground and the Vuvlo_on threshold is defined by the internal level.

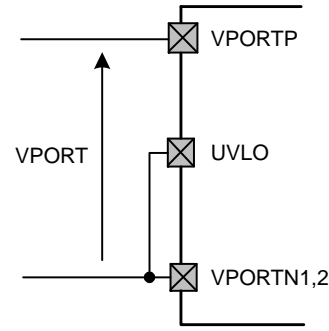


Figure 5. Default Internal UVLO Configuration (NCP1093 only)

To define the UVLO threshold externally, the UVLO pin must be connected to the center of an external resistor divider between VPORTP and VPORTN as shown in Figure 6.

In order to guarantee the detection signature, the equivalent input resistor made of the Ruvlo1, Ruvlo2 and Rdet should be equal to 24.9 kΩ.

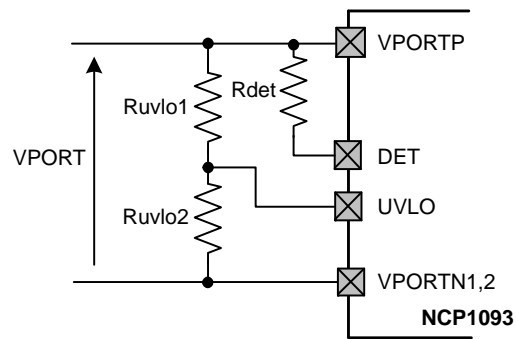


Figure 6. Default Internal UVLO Configuration (NCP1093 only)

For a Vuvlo_on desired turn-on voltage threshold, Ruvlo1 and Ruvlo2 can be calculated using the following equations:

$$R_{uvlo} = \frac{24.9 \text{ k} \cdot R_{det}}{R_{det} - 24.9 \text{ k}}$$

with $R_{uvlo1} + R_{uvlo2} = R_{uvlo}$

and $R_{uvlo2} = \frac{1.2}{V_{uvlo_on}} \cdot R_{uvlo}$

With:

Vuvlo_on: Desired Turn-On voltage threshold

Example for a Targeted U_{vlo_on} of 35 V:

Let's start with a R_{det} of 30.1 k Ω . This gives a R_{vlo} of 144 k Ω made with a R_{vlo2} of 4.99 k Ω and a R_{vlo1} of 140 k Ω (closest values from E96 series). Note that there is a pull down current of 2.5 μ A typ on the UVLO. Assuming the previous example, this pull down current will create a (non critical) systematic offset of 350 mV on the U_{vlo_on} level of 35 V.

The external UVLO hysteresis on the NCP1093 is about 15 percent typical.

Inrush and Operational Current Limitations

Both inrush and operational current limit are defined by an external R_{inrush} resistor connected between INRUSH and VPORTN. The low inrush current limit allows smooth charge of large dc-dc converter input capacitor by limiting the power dissipation over the internal pass switch. In power mode, the operational current limit protects the pass switch

and the PD application against excessive transient current and failure on the dc-dc converter output.

Once the input supply reached the U_{vlo_on} level, the charge of C_{pd} capacitor starts with a current limitation set to the INRUSH level. When this capacitor is fully charged, the current limit switches without any spikes from the inrush current to the operational current level and the power good indicator on PGOOD pin is turned on. The capacitor is considered to be fully charged once the following conditions are satisfied:

1. The drain-source voltage of the Pass Switch has decreased below the $V_{ds_pgood_on}$ level (typical 1 V)
2. The gate-source voltage of the Pass Switch is sufficiently high (above 2 V typical) which means the current in the pass switch has decreased below the current limit.

This mechanism is depicted in the following Figure 7.

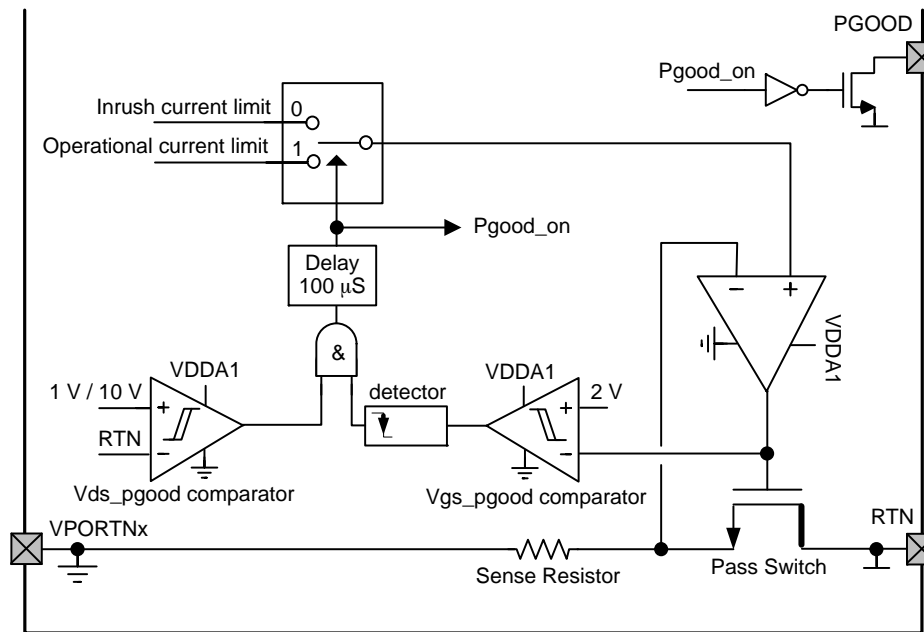


Figure 7. Inrush and Operational Current Limitation Selection Mechanism

The operational current limit and the power good indicator stays active as long as R_{TN} voltage stays below the $v_{ds_pgood_off}$ threshold (10 V typical) and the input supply stay above the U_{vlo_off} level. Therefore, fast and large voltage step lower than 10 V are tolerated on the input without interruption of the converter controller. Higher input transient will not affect the behavior if R_{TN} does not exceed 10 V for more than 100 μ s. Such input voltage steps may be introduced by a PSE which is switched to a higher power supply. In case R_{TN} is still above 10 V after this delay, the power good is turned off and the pass switch current limit falls back to the inrush level.

PGOOD Indicator

The NCP1093/94 integrate a Power Good indicator circuitry indicating the end of the dc-dc converter input capacitor charge, and the enabling of the operational current limit. This indicator is implemented on the PGOOD pin which goes in open drain state when active and which is pulled to ground during turn off.

A possible usage of this PGOOD pin is illustrated in Figure 8. During the inrush phase, the converter controller is forced in standby mode due to the PGOOD pin forcing low the under voltage lock out pin of the controller. Once the C_{pd} capacitor is fully charged, PGOOD goes in open drain state, allowing the start up sequence of the converter controller.

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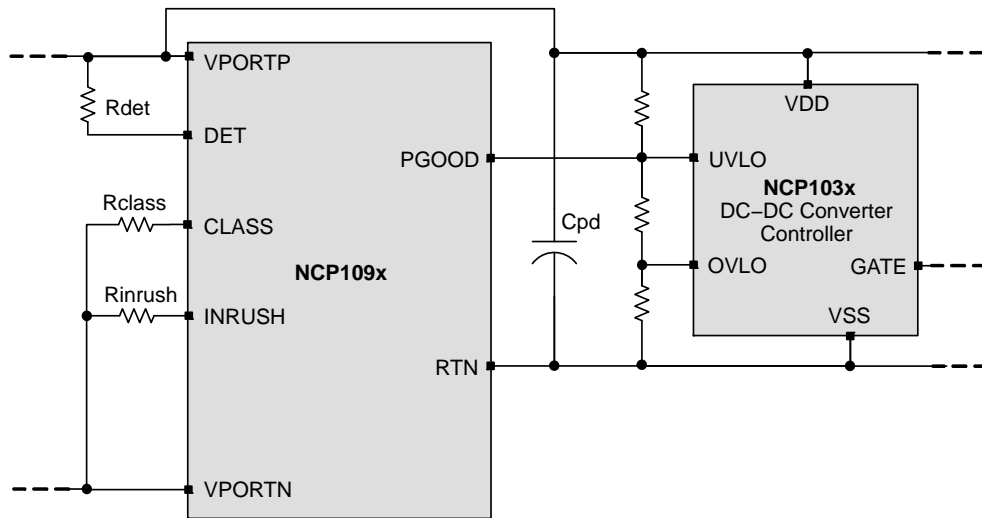


Figure 8. Power GOOD Implementation

NCLASS_AT Dual Event Classification Indicator

The *nCLASS_AT* active low open drain output pin should be used to notify to the microprocessor of the Powered Device that the PSE did a one or two event Hardware Classification.

If a 2 event Hardware classification has been done and once the PD application power has been applied, the

nCLASS_AT will be pulled low to RTN (ground connection of the DC/DC controller converter).

Otherwise, *nCLASS_AT* will be in high impedance mode.

The following Scheme illustrates how the *nCLASS_AT* pin may be configured with the processor of the Powered Device. An optocoupler is here used to guarantee to the full isolation between the cable and the application.

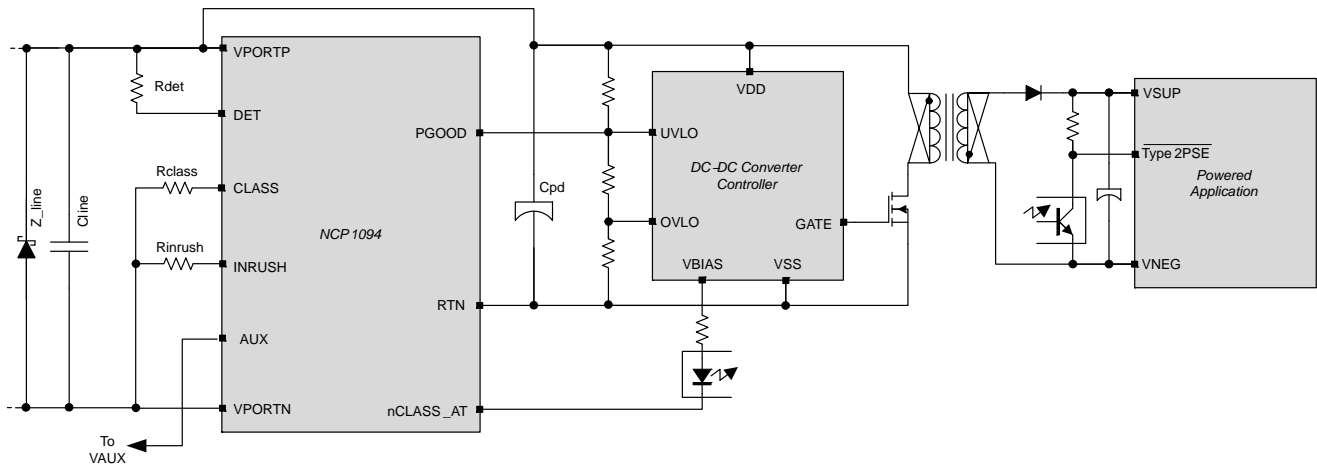


Figure 9. nClass AT indicator / possible implementation with the Powered Device

As soon as the application is powered by the DC/DC and after its initialization, the microprocessor will check if the PD interface detected a 2 event hardware classification by reading its digital input (*INI* in this example). If this *INI* pin is low, the application knows that the type 2 PSE, and therefore it can consume power till the level specified by the IEEE802.3at standard. Otherwise the application will have to perform a Layer 2 classification with the PSE.

Hereafter are described several scenarios for which the NCP109x will not enable its *nCLASS_AT* pin during the Powered Mode:

- ◆ The PSE skipped the classification phase
- ◆ The PSE did a 1 event hardware classification (it can be a type 1 PSE or a type 2 PSE with Layer 2 only)
- ◆ The PSE did a 2 event hardware classification but it didn't well control the input voltage in the Mark voltage (it crossed the Reset range for example).

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Auxiliary Supply

To support application connected to non-PoE enabled networks and minimize the bill of materials, the NCP1094 supports drawing power from an external supply and allows simplified designs with PoE or auxiliary supply priorities.

In most of the cases, the auxiliary supply is connected between VPORTP and RTN with a serial diode between VPORTP and VAUX, as shown in Figure 10.

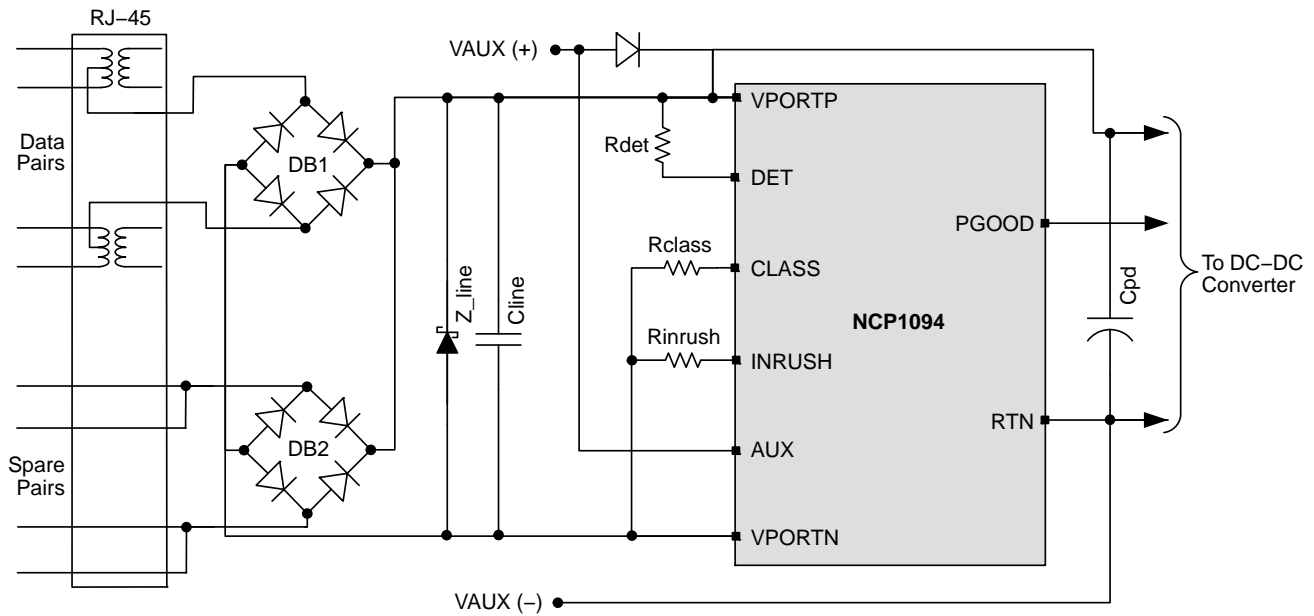


Figure 10. Auxiliary Supply Dominant PD Interface

The NCP1094 offers an AUX input pin which turns off the pass switch when pulled high. This feature is useful for PD applications where the auxiliary supply has to be dominant over the PoE supply. When the auxiliary supply is inserted on a POE powered application, the pass switch disconnection will move the current path from the PSE to the rear auxiliary supply. Since the current delivered by the PSE will go below the DC MPS level (specified in IEEE 802.3 af/at standard), the PSE will disconnect the PoE-PD

and the application will remain supplied by the auxiliary supply. The transition will happen without any power conversion interruption since the PGOOD indicator stays active (high impedance state).

Figure 11 depicts an other PD application where the POE supply is dominant over the VAUX supply. A diode D1 has been added in order to not corrupt the PD detection signature when the dc-dc converter is supplied by VAUX.

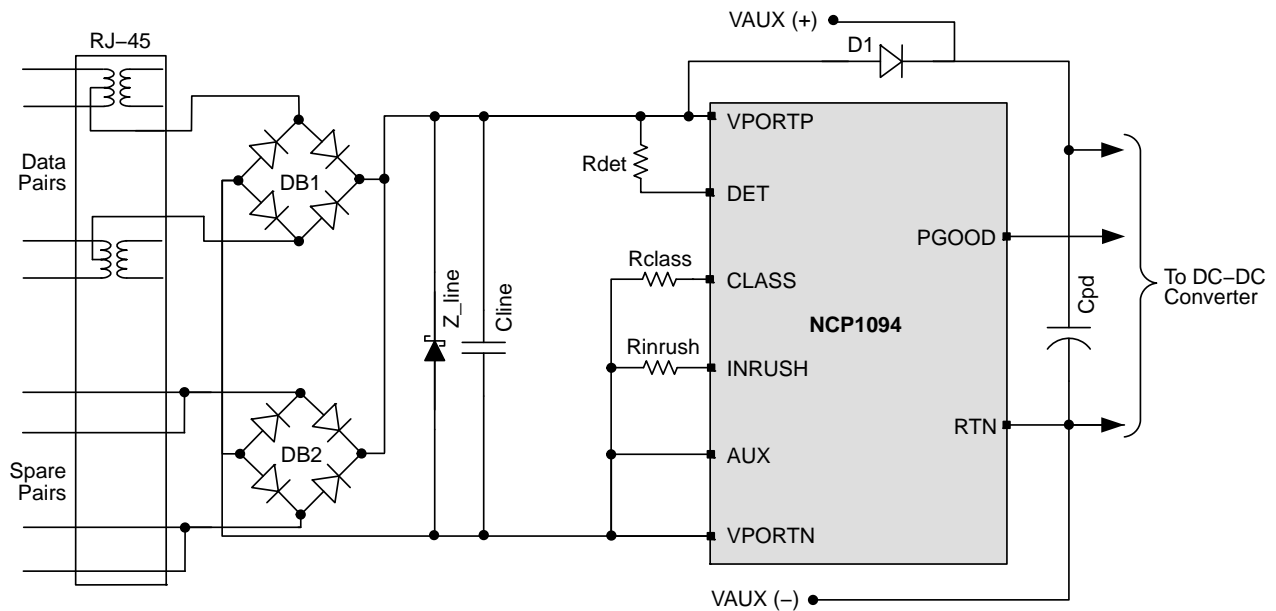


Figure 11. PoE Supply Dominant PD Interface

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Thermal Shutdown

The NCP1093/94 include a thermal shutdown which protect the device in case of high junction temperature. Once the thermal shutdown (TSD) threshold is exceeded, the classification block, the pass switch and the PGOOD indicator are disabled. The NCP109X returns automatically to normal operation once the die temperature has fallen below the TSD low limit.

Company or Product Inquiries

For more information about ON Semiconductor's Power over Ethernet products visit our Web site at <http://www.onsemi.com>.

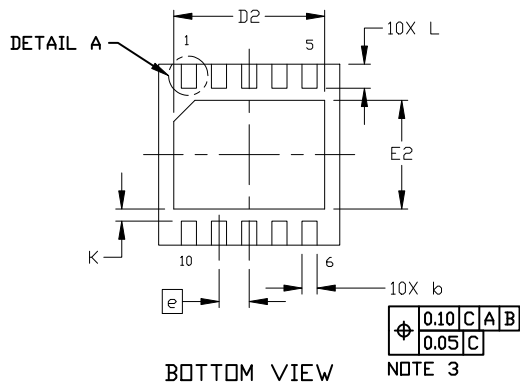
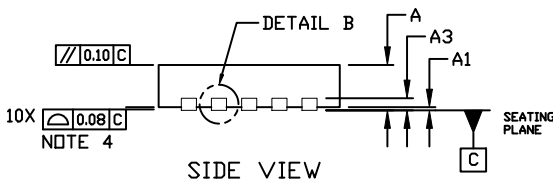
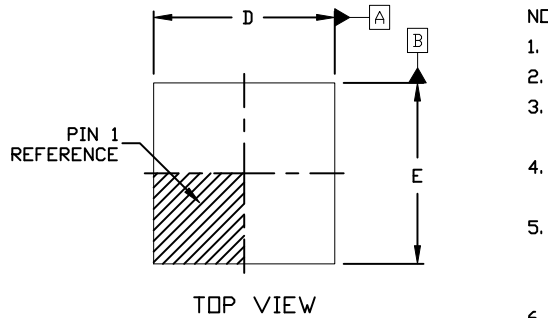
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

DFN10, 3x3, 0.5P CASE 485C ISSUE F

DATE 16 DEC 2021



GENERIC MARKING DIAGRAM*



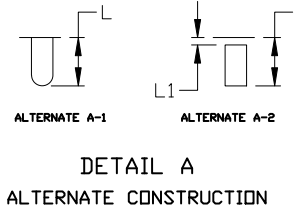
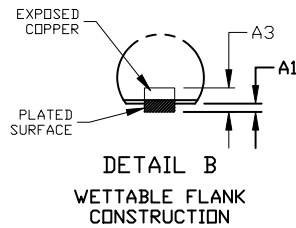
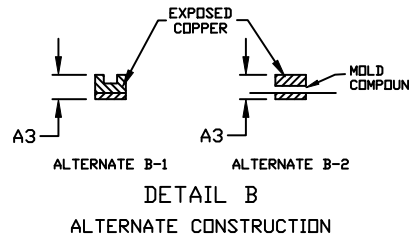
- XXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

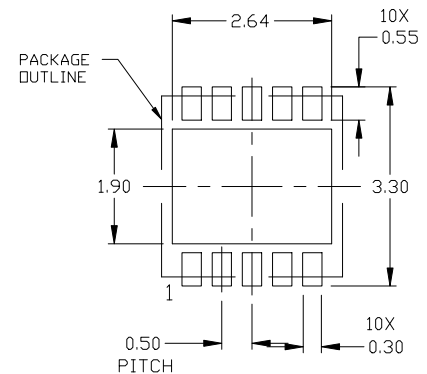
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSION AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL *b* MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASH MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL.
6. FOR DEVICE OPN CONTAINING W OPTION, DETAIL A AND DETAIL B ALTERNATE CONSTRUCTIONS ARE NOT APPLICABLE. WETTABLE FLANK CONSTRUCTION IS DETAIL B AS SHOWN ON SIDE VIEW OF PACKAGE.



| DIM | MILLIMETERS | | |
|----------|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0.00 | --- | 0.05 |
| A3 | 0.20 REF | | |
| <i>b</i> | 0.18 | 0.23 | 0.30 |
| D | 2.90 | 3.00 | 3.10 |
| D2 | 2.40 | 2.50 | 2.60 |
| E | 2.90 | 3.00 | 3.10 |
| E2 | 1.70 | 1.80 | 1.90 |
| <i>e</i> | 0.50 BSC | | |
| K | 0.20 REF | | |
| L | 0.30 | 0.40 | 0.50 |
| L1 | --- | --- | 0.03 |



RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|-------------------------|------------------------------------|--|
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| DESCRIPTION: | DFN10, 3X3 MM, 0.5 MM PITCH | PAGE 1 OF 1 |

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