

# NCP512

## Voltage Regulator - CMOS, Low Iq

### 80 mA

The NCP512 series of fixed output linear regulators are designed for handheld communication equipment and portable battery powered applications which require low quiescent. The NCP512 series features an ultra-low quiescent current of 40  $\mu$ A. Each device contains a voltage reference unit, an error amplifier, a PMOS power transistor, resistors for setting output voltage, current limit, and temperature limit protection circuits.

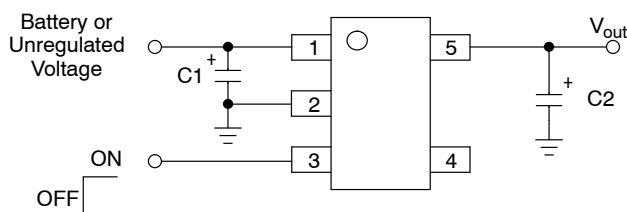
The NCP512 has been designed to be used with low cost ceramic capacitors. The device is housed in the micro-miniature SC70-5 surface mount package. Standard voltage versions are 1.3, 1.5, 1.8, 2.2, 2.5, 2.7, 2.8, 3.0, 3.1, 3.3, and 5.0 V. Other voltages are available in 100 mV steps.

#### Features

- Low Quiescent Current of 40  $\mu$ A Typical
- Low Dropout Voltage of 180 mV at 80 mA and 3.0 V  $V_{out}$
- Low Output Voltage Option
- Output Voltage Accuracy of 2.0%
- Industrial Temperature Range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
- These are Pb-Free Devices

#### Typical Applications

- Cellular Phones
- Battery Powered Consumer Products
- Hand-Held Instruments
- Camcorders and Cameras



This device contains 86 active transistors

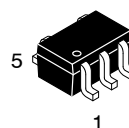
Figure 1. Typical Application Diagram



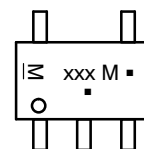
ON Semiconductor®

<http://onsemi.com>

#### MARKING DIAGRAM



SC70-5/SC-88A/  
SOT-353  
SQ SUFFIX  
CASE 419A



xxx = Device Code

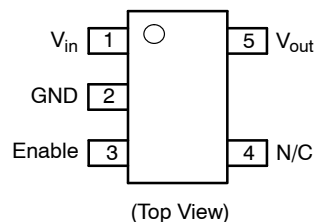
M = Date Code\*

▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and/or position may vary depending upon manufacturing location.

#### PIN CONNECTIONS



#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

# NCP512

## PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	V <sub>in</sub>	Positive power supply input voltage.
2	GND	Power supply ground.
3	Enable	This input is used to place the device into low-power standby. When this input is pulled low, the device is disabled. If this function is not used, Enable should be connected to V <sub>in</sub> .
4	N/C	No internal connection.
5	V <sub>out</sub>	Regulated output voltage.

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V <sub>in</sub>	0 to 6.0	V
Enable Voltage	Enable	-0.3 to V <sub>in</sub> + 0.3	V
Output Voltage	V <sub>out</sub>	-0.3 to V <sub>in</sub> + 0.3	V
Power Dissipation and Thermal Characteristics			
Power Dissipation	P <sub>D</sub>	Internally Limited	W
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	400	°C/W
Operating Junction Temperature	T <sub>J</sub>	+150	°C
Maximum Junction Temperature	T <sub>J(max)</sub>	+150	°C
Operating Ambient Temperature	T <sub>A</sub>	-40 to +85	°C
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- This device series contains ESD protection and exceeds the following tests:  
Human Body Model 2000 V per MIL-STD-883, Method 3015  
Machine Model Method 200 V
- Latch-up capability (85°C) ± 200 mA DC with trigger voltage.

# NCP512

**ELECTRICAL CHARACTERISTICS** ( $V_{in} = V_{out(nom.)} + 1.0\text{ V}$ ,  $V_{enable} = V_{in}$ ,  $C_{in} = 1.0\ \mu\text{F}$ ,  $C_{out} = 1.0\ \mu\text{F}$ ,  $T_J = 25^\circ\text{C}$ , unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ( $T_A = 25^\circ\text{C}$ , $I_{out} = 10\text{ mA}$ )	$V_{out}$				V
1.3 V		1.261	1.3	1.339	
1.5 V		1.455	1.5	1.545	
1.8 V		1.746	1.8	1.854	
2.2 V		2.134	2.2	2.266	
2.5 V		2.425	2.5	2.575	
2.7 V		2.646	2.7	2.754	
2.8 V		2.744	2.8	2.856	
3.0 V		2.94	3.0	3.06	
3.1 V		3.038	3.1	3.162	
3.3 V	3.234	3.3	3.366		
5.0 V	4.900	5.0	5.100		
Output Voltage ( $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ , $I_{out} = 10\text{ mA}$ )	$V_{out}$				V
1.3 V		1.261	1.3	1.339	
1.5 V		1.455	1.5	1.545	
1.8 V		1.746	1.8	1.854	
2.2 V		2.134	2.2	2.266	
2.5 V		2.425	2.5	2.575	
2.7 V		2.619	2.7	2.781	
2.8 V		2.716	2.8	2.884	
3.0 V		2.910	3.0	3.09	
3.1 V		3.007	3.1	3.193	
3.3 V	3.201	3.3	3.399		
5.0 V	4.900	5.0	5.100		
Line Regulation ( $I_{out} = 10\text{ mA}$ )	$Reg_{line}$				mV/V
1.3 V–4.4 V ( $V_{in} = V_{out(nom.)} + 1.0\text{ V}$ to 6.0 V)		–	1.0	3.0	
4.5 V–5.0 V ( $V_{in} = 5.5\text{ V}$ to 6.0 V)		–	1.0	3.0	
Load Regulation ( $I_{out} = 1.0\text{ mA}$ to 80 mA)	$Reg_{load}$	–	0.3	0.8	mV/mA
Output Current ( $V_{out} = (V_{out} \text{ at } I_{out} = 80\text{ mA}) - 3\%$ )	$I_{o(nom.)}$				mA
1.3 V–3.9 V ( $V_{in} = V_{out(nom.)} + 2.0\text{ V}$ )		80	200	–	
4.0 V–5.0 V ( $V_{in} = 6.0\text{ V}$ )		80	200	–	
Dropout Voltage ( $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ , $I_{out} = 80\text{ mA}$ , Measured at $V_{out} = V_{out(nom)} - 3.0\%$ )	$V_{in} - V_{out}$				mV
1.3 V		–	520	700	
1.5 V		–	450	550	
1.8 V		–	350	450	
2.2 V		–	240	300	
2.5 V		–	220	300	
2.7 V		–	200	300	
2.8 V		–	200	300	
3.0 V		–	180	300	
3.1 V		–	170	300	
3.3 V	–	160	300		
5.0 V	–	120	300		
Ground Current (Enable Input = $V_{in}$ , $I_{out} = 1.0\text{ mA}$ to $I_{o(nom.)}$ )	$I_{GND}$	–	40	90	$\mu\text{A}$
Quiescent Current ( $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ )	$I_Q$				$\mu\text{A}$
(Enable Input = 0 V)		–	0.1	1.0	
(Enable Input = $V_{in}$ , $I_{out} = 1.0\text{ mA}$ to $I_{o(nom.)}$ )		–	40	90	
Output Short Circuit Current ( $V_{out} = 0\text{ V}$ )	$I_{out(max)}$				mA
1.3 V–3.9 V ( $V_{in} = V_{out(nom.)} + 2.0\text{ V}$ )		150	250	400	
4.0 V–5.0 V ( $V_{in} = 6.0\text{ V}$ )		150	250	400	
Output Voltage Noise ( $f = 100\text{ Hz}$ to $100\text{ kHz}$ , $I_{out} = 30\text{ mA}$ , $C_{out} = 1\ \mu\text{F}$ )	$V_n$	–	180	–	$\mu\text{V}_{RMS}$
Ripple Rejection ( $f = 1.0\text{ kHz}$ , 60 mA)	RR	–	50	–	dB
Enable Input Threshold Voltage	$V_{th(en)}$				V
(Voltage Increasing, Output Turns On, Logic High)		1.3	–	–	
(Voltage Decreasing, Output Turns Off, Logic Low)		–	–	0.3	
Output Voltage Temperature Coefficient	$T_C$	–	$\pm 100$	–	ppm/ $^\circ\text{C}$

3. Maximum package power dissipation limits must be observed.

$$PD = \frac{T_J(max) - T_A}{R_{\theta JA}}$$

4. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

# NCP512

## TYPICAL CHARACTERISTICS

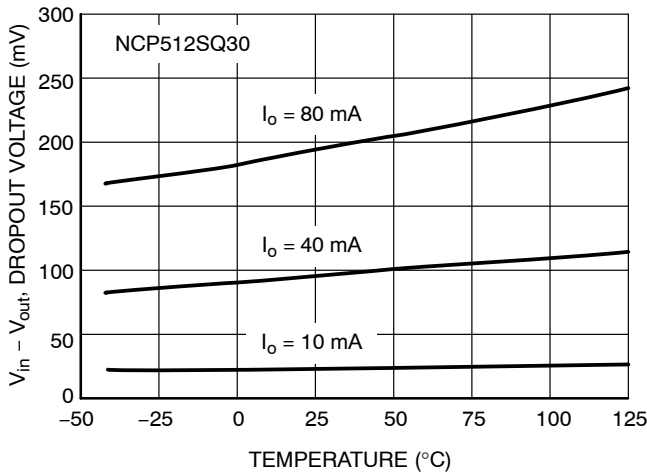


Figure 2. Dropout Voltage vs. Temperature

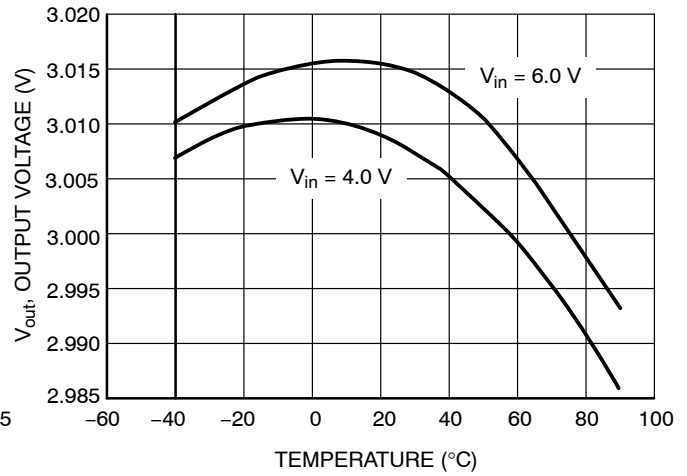


Figure 3. Output Voltage vs. Temperature

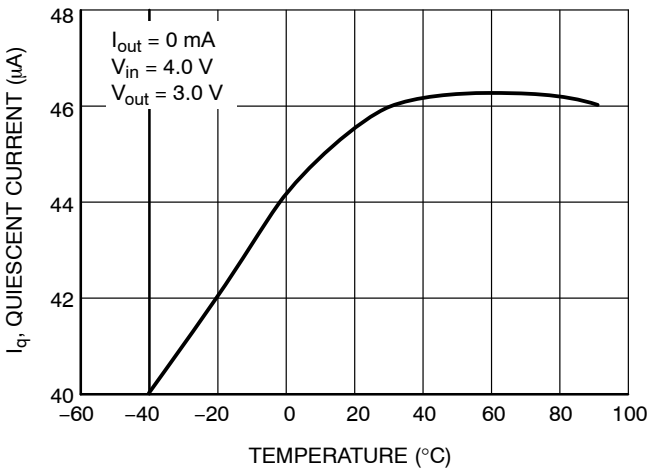


Figure 4. Quiescent Current vs. Temperature

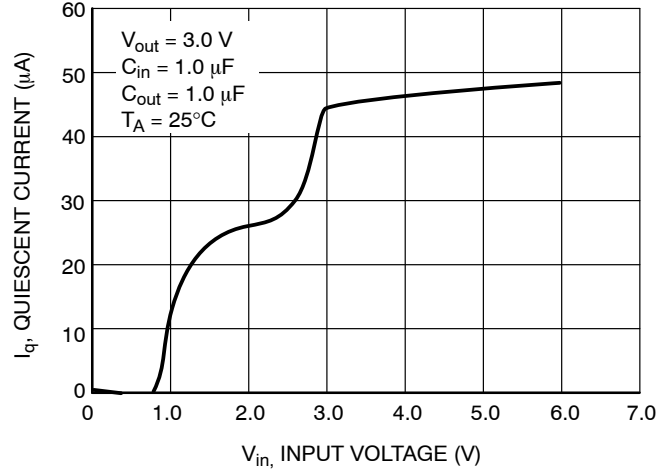


Figure 5. Quiescent Current vs. Input Voltage

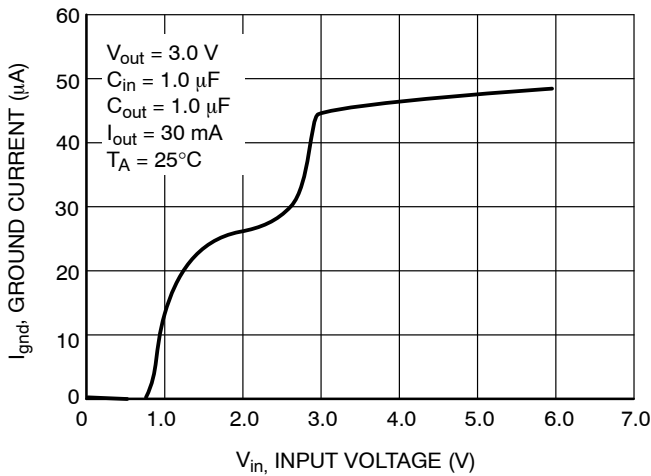


Figure 6. Ground Pin Current vs. Input Voltage

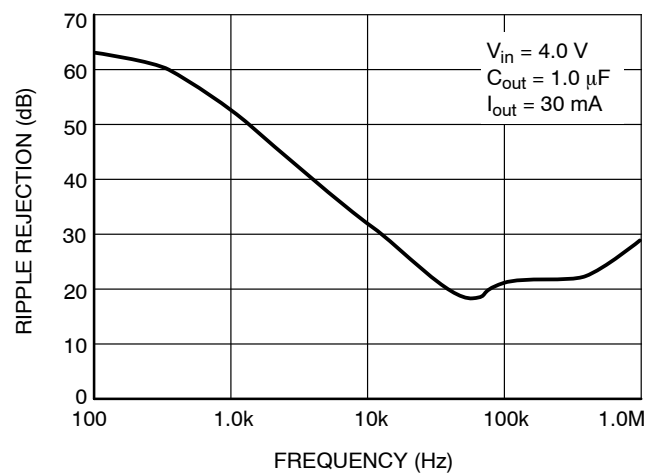


Figure 7. Ripple Rejection vs. Frequency

# NCP512

## TYPICAL CHARACTERISTICS

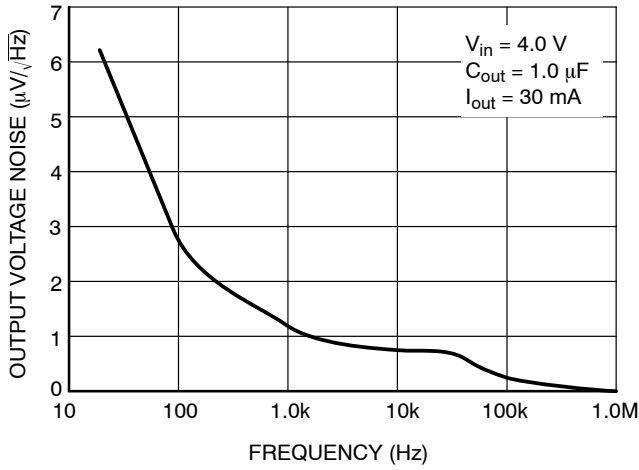


Figure 8. Output Noise Density

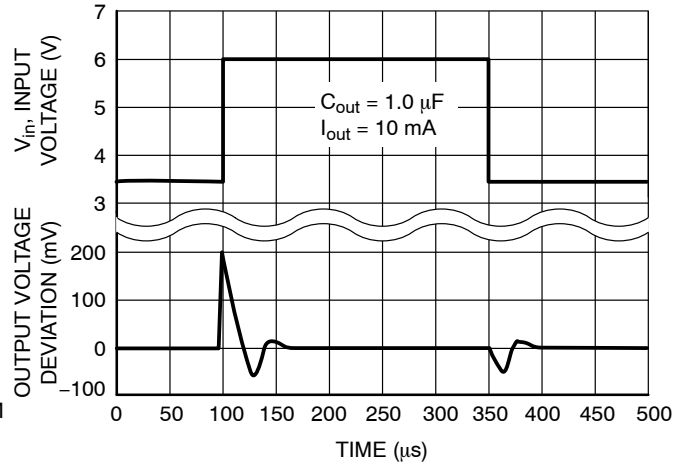


Figure 9. Line Transient Response

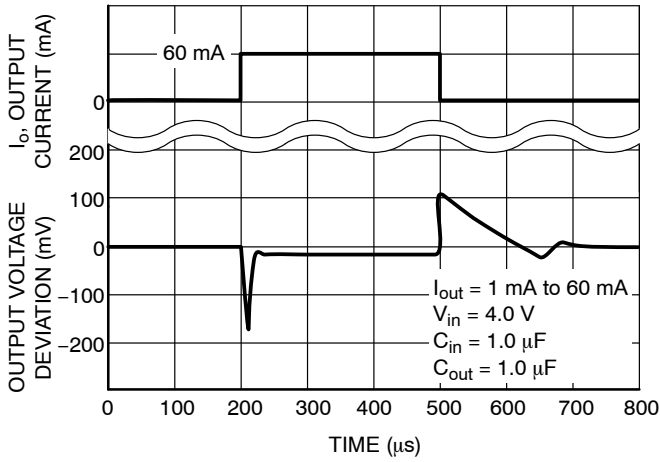


Figure 10. Load Transient Response

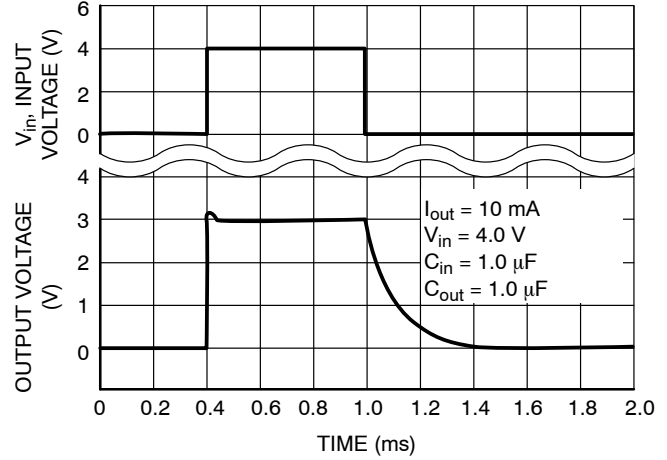


Figure 11. Turn-on Response

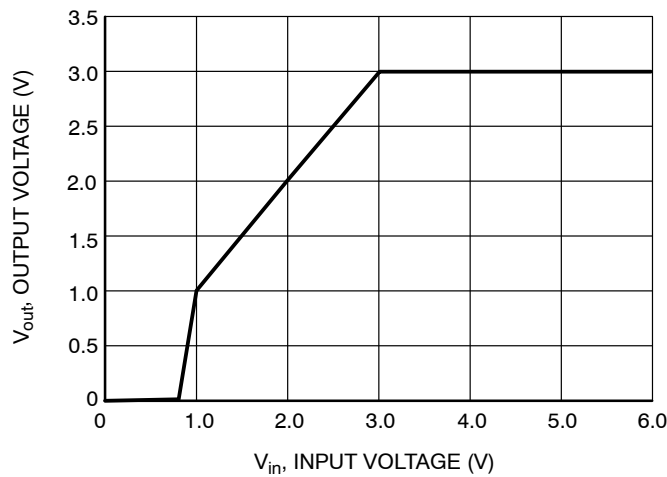


Figure 12. Output Voltage vs. Input Voltage

## DEFINITIONS

### **Load Regulation**

The change in output voltage for a change in output current at a constant temperature.

### **Dropout Voltage**

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 3.0% below its nominal. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

### **Maximum Power Dissipation**

The maximum total dissipation for which the regulator will operate within its specifications.

### **Quiescent Current**

The quiescent current is the current which flows through the ground when the LDO operates without a load on its output: internal IC operation, bias, etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

### **Line Regulation**

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse technique such that the average chip temperature is not significantly affected.

### **Line Transient Response**

Typical over and undershoot response when input voltage is excited with a given slope.

### **Thermal Protection**

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 160°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

### **Maximum Package Power Dissipation**

The maximum power package dissipation is the power dissipation level at which the junction temperature reaches its maximum operating value, i.e. 125°C. Depending on the ambient power dissipation and thus the maximum available output current.

# NCP512

## APPLICATIONS INFORMATION

A typical application circuit for the NCP512 series is shown in Figure 1, front page.

### Input Decoupling (C1)

A 1.0  $\mu\text{F}$  capacitor either ceramic or tantalum is recommended and should be connected close to the NCP512 package. Higher values and lower ESR will improve the overall line transient response.

TDK capacitor: C2012X5R1C105K, or C1608X5R1A105K

### Output Decoupling (C2)

The NCP512 is a stable regulator and does not require any specific Equivalent Series Resistance (ESR) or a minimum output current. Capacitors exhibiting ESRs ranging from a few  $\text{m}\Omega$  up to  $5.0\ \Omega$  can thus safely be used. The minimum decoupling value is 1.0  $\mu\text{F}$  and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum capacitors. Larger values improve noise rejection and load regulation transient response.

TDK capacitor: C2012X5R1C105K, C1608X5R1A105K, or C3216X7R1C105K

### Enable Operation

The enable pin will turn on the regulator when pulled high and turn off the regulator when pulled low. These limits of threshold are covered in the electrical specification section of this data sheet. If the enable is not used then the pin should be connected to  $V_{in}$ .

### Hints

Please be sure the  $V_{in}$  and GND lines are sufficiently wide. When the impedance of these lines is high, there is a chance to pick up noise or cause the regulator to malfunction.

Set external components, especially the output capacitor, as close as possible to the circuit, and make leads as short as possible.

### Thermal

As power across the NCP512 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material and also the ambient temperature effect the rate of temperature rise for the part. This is stating that when the NCP512 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power dissipation applications.

The maximum dissipation the package can handle is given by:

$$PD = \frac{T_{J(\text{max})} - T_A}{R_{\theta JA}}$$

If junction temperature is not allowed above the maximum  $125^\circ\text{C}$ , then the NCP512 can dissipate up to 250 mW @  $25^\circ\text{C}$ .

The power dissipated by the NCP512 can be calculated from the following equation:

$$P_{\text{tot}} = [V_{in} * I_{\text{gnd}}(I_{\text{out}})] + [V_{in} - V_{\text{out}}] * I_{\text{out}}$$

or

$$V_{in\text{MAX}} = \frac{P_{\text{tot}} + V_{\text{out}} * I_{\text{out}}}{I_{\text{gnd}} + I_{\text{out}}}$$

If an 80 mA output current is needed then the ground current from the data sheet is  $40\ \mu\text{A}$ . For an NCP512 (3.0 V), the maximum input voltage will then be 6.12 V.

# NCP512

## ORDERING INFORMATION

Device	Nominal Output Voltage*	Marking	Package	Shipping†
NCP512SQ13T1G	1.3	LIW	SC-88A (SOT-353) (Pb-Free)	3000 Units/ 7" Tape & Reel
NCP512SQ13T2G				
NCP512SQ15T1G	1.5	LCK		
NCP512SQ15T2G				
NCP512SQ18T1G	1.8	LCL		
NCP512SQ18T2G				
NCP512SQ22T1G	2.2	LIA		
NCP512SQ22T2G				
NCP512SQ25T1G	2.5	LCM		
NCP512SQ25T2G				
NCP512SQ27T1G	2.7	LCN		
NCP512SQ27T2G				
NCP512SQ28T1G	2.8	LCO		
NCP512SQ28T2G				
NCP512SQ30T1G	3.0	LCP		
NCP512SQ30T2G				
NCP512SQ31T1G	3.1	LFO		
NCP512SQ31T2G				
NCP512SQ33T1G	3.3	LCQ		
NCP512SQ33T2G				
NCP512SQ50T1G	5.0	LCR		
NCP512SQ50T2G				

\*Additional voltages in 100 mV steps are available upon request by contacting your ON Semiconductor representative.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.





SCALE 2:1

SC-88A (SC-70-5/SOT-353)  
CASE 419A-02  
ISSUE M

DATE 11 APR 2023



RECOMMENDED MOUNTING FOOTPRINT

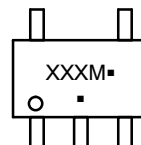
\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3	0.20 REF		
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30

GENERIC MARKING DIAGRAM\*



\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

STYLE 1:

- PIN 1. BASE
- 2. EMITTER
- 3. BASE
- 4. COLLECTOR
- 5. COLLECTOR

STYLE 2:

- PIN 1. ANODE
- 2. EMITTER
- 3. BASE
- 4. COLLECTOR
- 5. CATHODE

STYLE 3:

- PIN 1. ANODE 1
- 2. N/C
- 3. ANODE 2
- 4. CATHODE 2
- 5. CATHODE 1

STYLE 4:

- PIN 1. SOURCE 1
- 2. DRAIN 1/2
- 3. SOURCE 1
- 4. GATE 1
- 5. GATE 2

STYLE 5:

- PIN 1. CATHODE
- 2. COMMON ANODE
- 3. CATHODE 2
- 4. CATHODE 3
- 5. CATHODE 4

STYLE 6:

- PIN 1. EMITTER 2
- 2. BASE 2
- 3. EMITTER 1
- 4. COLLECTOR
- 5. COLLECTOR 2/BASE 1

STYLE 7:

- PIN 1. BASE
- 2. EMITTER
- 3. BASE
- 4. COLLECTOR
- 5. COLLECTOR

STYLE 8:

- PIN 1. CATHODE
- 2. COLLECTOR
- 3. N/C
- 4. BASE
- 5. EMITTER

STYLE 9:

- PIN 1. ANODE
- 2. CATHODE
- 3. ANODE
- 4. ANODE
- 5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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DESCRIPTION:	SC-88A (SC-70-5/SOT-353)	PAGE 1 OF 1

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